



Appendix E2

3COM IBIS MODEL STANDARD

APPROVALS

<i>TITLE</i>	<i>NAME</i>	<i>SIGNATURE & DATE</i>
Mgr, Hardware Engineering	Steve A. Martin	s/ 9/14/1999
Sr. Signal Integrity Engineer	Mohammad Ali	s/ 9/14/1999
Sr. Signal Integrity Engineer	Roy Leventhal	s/ 9/14/1999
SEPG	David Baker	s/ 9/14/1999
Publishing Services Release	Karen Lin	s/ 9/15/1999

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1. Purpose

This document defines the guidelines that an IBIS model should meet for 3Com's use.

This document establishes a check and balance system which will insure that new IBIS models used in 3Com products meet or exceed the design, quality, reliability, procurement, and production requirements of 3Com.

Possession of accurate IBIS data and a good software tool to simulate high speed digital signal integrity performance significantly enhances the productivity of 3Com's design process and can mean the difference between product success and failure.

Industry compliance to the IBIS standards referred to below is voluntary and cannot be depended upon to ensure 3Com's interests. The IBIS standard underlies this standard. In addition this standard would underlie a part-specific purchase specification for an IBIS model for the part should 3Com require one.

This standard outlines minimum 3Com requirements regarding IBIS model quality based on the IBIS definitions and requirements outlined herein and in the IBIS specification.

In addition, a part-specific IBIS model purchase specification may require more model properties than are required to meet our minimum standard. These add-on options are at the discretion of the Hardware Design Engineer. By definition, they (as well as the minimum standard properties) fall under, and are defined by the IBIS specification version from the EIA Committee that is referenced in the purchase specification.

Four companion documents, "**Simulation Model Procurement Process (E0167)**," "**Simulation Model Creation and Updating Process (E0171)**," "**Simulation Model Verification Process (E0172)**" and "**How to Use the IBIS Model**" offer guidelines for adding additional IBIS data requirements for detail, accuracy and precision. A Hardware Design Engineer may need to supplement the minimum standard herein based on challenges in meeting design objectives.

2. Scope

This standard applies to all IBIS models entered into the 3Com CSBU Library.

3. Definitions

Specification - A written document or electronic equivalent that is relied upon to identify the mechanical and/or electrical parameters for a component.

IBIS - An acronym for "**Input/Output Buffer Information Specification.**" An IBIS model is not a true electrical model in the sense of a modeling language or a physical/electrical representation of an I/O buffer. An IBIS model is a file of data that conforms to a data exchange format, or the latest released version of that specification, agreed to in the electronics industry. Further, this specification allows for a great amount of freedom in interpretation by its users.

IBIS Open Forum - A committee first formed in May 1993 under the Electronic Industries Association (EIA) has been responsible for the updating, approval and release of this specification. IBIS is considered an emerging standard. As of this date, 8/15/99, it is at version 3.2.

IBIS Version 3.2, - Has been formally ratified as ANSI/EIA-656 January 15, 1999 as an international standard by the IEC (International Electrotechnical Commission) as IEC 62014-1.

Downloadable Copies – Copies of the IBIS specification and previous IBIS versions are downloadable from:

<ftp://ftp.eda.org/pub/ibis/>

Component - a constituent element of a 3COM Carrier product. Such elements include boxes, manuals, electrical and mechanical piece parts etc.

Package - Part of the physical structure of an electrical device usually used to describe the form factor and carrier for the electrical components, which make up the device. EX: 0805, SO14, HCU etc

4. Applicable Documents

ANSI/EIA (American National Standards Institute/Electronic Industries Association)

- 656 IBIS Version 3.2 or later current version, or:
- IEC (International Electrotechnical Commission) 62014-1 or later current version.
- IBIS Model Accuracy Specification - Draft 1.0

New Electrical Component Approval Process (E0001)

Component Additional Source Qualification Process (E0002)

Simulation Model Procurement Process (E0167)

Simulation Model Creation and Updating Process (E0171)

Simulation Model Verification Process (E0172)

Signal Integrity Simulation Process (Exxxx)

Design Guides:

IBIS Model Syntax

How to Use the IBIS Model

Signal Integrity - Board Design & Simulation Techniques

Signal Integrity - 101

Summary of Key [Keyword] IBIS 3.2 Enhancements:

(Si_location, Timing_location): Allows specification of where (die or pin) signal integrity and timing measurements are taken.

[Number Of Sections]: Adds multiple connection sections and forks for connections between pin and die. RLC elements allowed.

[Series Pin Mapping]: Adds series pin mappings, models and switching function table groups.

[Series Switch Groups]: Adds constructs that define allowable switching combinations (states) for series switches.

(Series or Series_switch added to Model_types): Adds constructs that define series RLC, Current and MOSFET elements for series switches.

[Model Selector]: Adds constructs for programmable drive strength buffers.

[Model Spec]: Adds constructs for describing hysteresis effects.

[Add Submodel]: Adds capability of adding special purpose function submodels to models.

[Submodel Spec]: Adds constructs for adding trigger voltages and delays; GND and POWER pulse tables. Allows dynamic clamping and bus_hold to be described.

[Driver Schedule]: Adds relative switching sequence description to produce multi-stage drive, soft turn-on, etc.

[TTgnd], [TTpower]: Adds constructs for diode transit time and estimating capacitance loading of clamps.

[Begin Board Description]: Adds constructs for describing (abstracting) board or substrate as a component.

Additional keywords necessary for supporting these new features were also added.

Note:

This document was updated to the IBIS 3.2 spec in August, 1999.

5. 3Com Requirements

There are six numbered tables in section 5. Most of these numbered tables are split into several subtables covering more than one page. They organize the many keywords, parameters and subparameters of the IBIS spec found in this standard into six main categories:

- Table 1: General IBIS Properties - "boilerplate."
- Table 2: IBIS Component Properties - supplier, voltage and temperature ranges.
- Table 3: IBIS Package and Pin Properties - connections and parasitics.
- Table 4: IBIS V-I Behavioral Properties - driver voltage-current capabilities, clamping, power bussing, model types, etc.
- Table 5: IBIS V-T Behavioral Properties - slew rates and switching speeds.
- Table 6: IBIS Electrical Board Description - abstracting a board as a component.

In following sections are two sets of tables that are organized along the same lines except that: Tables 8 to 13 point to my guesses as to the most likely sources of data, and; Tables 14 to 19 point to my guesses as to the most likely documents to verify model data against.

5.1. Requirements by Keyword and Sub Parameter

Table 1: General IBIS Properties

Keyword	Description	Minimum Requirement	Comments
[IBIS Ver]	Version of IBIS spec used in file. Must be the first keyword in any IBIS file. Comment lines can precede	IBIS-Yes 3Com-Yes	Don't confuse with [File Rev]
[Comment Char]	For defining a new comment character	Optional	The standard IBIS comment character is a “ ” (pipe)
[File Name]	Name of the model file. 8 ascii lowercase characters max.	IBIS-Yes 3Com-Yes	Must end in .ibs extension
[File Rev]	Revision number of the model file	IBIS-Yes 3Com-Yes	Revision numbers must have meaning
[Date]	Date created or last revised	Optional	
[Source]	Originator of IBIS file	Optional	
[Notes]		Optional	Explanations & comments
[Copyright]		Optional	“ - - all rights reserved - - “
[Disclaimer]		Optional	Usually “- - for modeling only - - not guaranteed - - “

Table 2: IBIS Component Properties

Keyword	Description	Minimum Requirement	Comments
[Component]	Name of the component modeled. Each section begins with a new Component] keyword if the .ibs file contains data for more than one component.	IBIS-Yes 3Com-Yes	Beginning of the IBIS description. If several components are in one file, each must have its own [Component] section.
Si_location	Used to specify where (pin or die) SI measurements are taken.	Optional	Default is at the pin. Sub parameter of [Component]
Timing_location	Used to specify where (pin or die) timing measurements are taken.	Optional	Default is at the pin. Sub parameter of [Component]
[Manufacturer]	Maker of the component	IBIS-Yes 3Com-Yes	Second sources might have models different from first source and usually do
[Voltage Range]	Power supply voltage with tolerance. Range over which model operates.	IBIS-Yes 3Com-Yes	
[Temperature Range]	Actual die temperature range in measurements. Default 0/50/100 C°	IBIS-Yes 3com-Yes	If different than default values

Table 3: IBIS Package and Pin Properties

Keyword	Description	Minimum Requirement	Comments
[Package]	Default R_pkg, L_pkg, C_pkg parasitics applied globally to all component pins.	IBIS-Yes 3Com-Yes	Note 1
[Pin]	Associates the component's various I/O models to its external pins and signal names. Parameter values here override defaults in [Package]. All pins are supposed to be specified with a [Model] name.	IBIS-Yes 3Com-Yes	R_pin, C_pin, L_pin ¹ can be particularized to a pin and are often optionally supplied. Pins can be specified with POWER, GND or NC (no connect)
Signal_name	Sub parameters of [Pin] from same in data book	IBIS-Yes 3Com-Opt	SubParm of [Pin]. Often missing.
Model_name	Sub parameters of [Pin] name of I/O type for that pin	IBIS-Yes 3Com-Yes	SubParm of [Pin]. Often missing, but essential
R_pin, C_pin, L_pin	Sub parameters of [Pin]. Note 2.	IBIS-Yes 3Com-Yes	SubParm of [Pin]. Often missing, but important

(Table 3 cont.)

Note 1:

Typical values must be specified. If min & max are missing they must be noted with 'NA.'

Note 2:

Rpin, R_pin, R_pkg, Rpkg, Rdut and R_dut are all "equivalent." Likewise, C_pin, etc., L_pin, etc. But, Rpin, etc., allows for parasitic values specific to a pin and overrides Rpkg & Rdut when present.

¹ Under the [Pin] keyword the first additional level of detail in pin parasitics (beyond default package parasitics) is spelled out.

Table 3: IBIS Package and Pin Properties (cont.)

Keyword	Description	Minimum Requirement	Comments
[Package Model]	Name of the package model, if supplied. Can be supplied in a separate .pkg file if in the same directory as the .ibs file. Use [Package Model] within [Component] to show which package model is supplied with that component.	Optional	Package models allow for pin-pin coupling parasitics, ² etc. Overrides defaults in [Package]
[Define Package Model]		IBIS-Y-if 3Com-Y-if	Required if [Package Model] used
[Manufacturer]	Manufacturer of the parts that use this package	Note 3	
[OEM]	Manufacturer of the package	Note 3	
[Description]	Human readable package description	Note 3	
[Number of Pins]	Tells parser how many pins to expect	Note 3	

(Table 3 cont.)

Note 3:

Required (IBIS & 3Com) if [Define Package Model] used

² Under the [Package] keyword the second additional level of detail in pin parasitics (beyond individual pin parasitics) is spelled out.

Table 3: IBIS Package and Pin Properties (cont.)

Keyword	Description	Minimum Requirement	Comments
[Pin Numbers]	The ordered arrangement of the pin numbers	Note 3	
[Number Of Sections]	Defines the maximum number of sections that make up a package stub. A package stub is the connection between pin and pad.	Optional	Used to describe other interconnect than a single, lumped L/R/C for a pin.
Len	Length of a package stub section	Note 12	Given in terms of arbitrary units
L	Inductance of a package stub section	Note 12	Given in terms of "inductance/unit length"
R	Resistance of a package stub section	Note 12	ibid
C	Capacitance of a package stub section	Note 12	ibid
Fork	Indicates that the sections following, and up to Endfork, are part of a branch off the main package stub.	Note 12	
Endfork	End of the fork, or branch.	Note 12	Each Fork must have a corresponding Endfork

(Table 3 cont.)

Note 12:

Subparameter of [Pin Numbers]. These are the properties for each section of the stub on a pin in a package. For example, if the length of the section is 2 'units' and the inductance is 1.5 nh / unit, then the inductance of the section is 3.0 nh. If a Len of zero is specified then the L/R/C values are the total for the section. If $Len \neq 0$, then the total L/R/C for that section is multiplied by that value. However, then the L/R/C should be treated as distributed elements.

A package stub can include, but is not limited to, the pad to pin bondwire. A package stub begins at the connection to the die and ends at the point where the package pin interfaces with the board or substrate the package IC is mounted on.

Table 3: IBIS Package and Pin Properties (cont.)

Keyword	Description	Minimum Requirement	Comments
[Model Data]	Begins RLGC matrices which override [Pin] & [Package] parasitic element defaults	Optional	Model I/O cell assignments (types) are still controlled by [Pin]. Note 7.
[Resistance Matrix]	A 1x1 matrix is self-resistance of a single line, a 2x2 matrix is self and mutual resistances of 2 coupled lines, etc. The a_{11} , etc., elements are “self.” The a_{13} , etc., elements are “mutual.”	Note 7	The R, L & C matrices (G elements are usually zero or neglected) form the basis of coupled line (or connector or package) structures and all transmission lines.
[Inductance Matrix]	Ibid	Note 7	Ibid
[Capacitance Matrix]	Ibid	Note 7	ibid
[Row]	Used to denote the start of a new row in a matrix when the rows are more than 80 characters long.	Optional	
[Bandwidth]	The distance, in number of matrix elements on either side of the main diagonal, i.e. “band” beyond which the matrix elements are guaranteed to be zero. I.e., no significant coupling	Optional	Yes, if Banded_matrix matrices used. See “Creating an IBIS Model”
Banded_matrix	Subparameters of R, L & C matrices. A type of matrix.	Optional	Used when a full matrix for a large BGA, etc., array would be unnecessarily huge
Sparse_matrix	Subparameters of R, L & C matrices. A type of matrix.	Optional	Ibid
Full_matrix	Subparameters of R, L & C matrices. A type of matrix.	Optional	Ibid
[End Model Data]	End of the model data description	Note 7	
[End Package Model]	Defines the end of the .pkg file	Note 7	

(Table 3 cont.)

Note 7:

There is little reason to use the [Package Model] keyword unless intending to include RLGC matrices. The G (conductance) matrix is almost always zero. The R matrix is often zero, and when included, is almost always the self-resistance of the pin. The C & L matrices contain the mutual coupling elements that are the chief motivation for using the [Package Model].

Table 3 (cont.): IBIS Package and Pin Properties

Keyword	Description	Minimum Requirement	Comments
[Pin Mapping]	Used to tell which power/ground busses a particular driver, receiver or terminator cell, or their elements, are connected to.	Optional	When present, the bus connections for every pin listed in the [Pin] section must be given.
Pulldown_ref	Sub parameter of [Pin Mapping]. Each pulldown bus has a unique name. To meet minimum ground /power bounce, devices are being supplied with several such pins. Connections are designed to minimize ground/power impedance & xtalk.	Optional	All entries with identical labels are assumed to be connected together. Each unique I/O pin must be connected to at least one pin whose model name is POWER or GND. Else, they are all NC.
Pullup_ref	Ibid		
Gnd_clamp_ref	Ibid		
Power_clamp_ref	Ibid		
[Rac]	Resistance of internal RC shunt termination	IBIS-Yes 3Com-Yes	If present in device
[Cac]	Capacitance of internal RC shunt termination		
[Rgnd]	Internal package resistance of ground pin if and only if [Model_type] is Terminator		
[Rpower]	Internal package resistance of power pin if and only if [Model_type] is Terminator		
[Diff Pin]	Associates differential pins and their threshold voltages and timing offsets.	IBIS-Yes 3Com-Yes	If present in device. See also Polarity in [Model].
inv_pin	Sub parameter of [Diff Pin]. The inverting pin of the pair.	IBIS-Yes 3Com-Yes	Yes, if [Diff Pin] used
Vdiff	Sub parameter of [Diff Pin]. Specified output or input threshold differential voltage.	Note 4	
tdelay_typ	Sub parameter of [Diff Pin]. Launch delay of the non-inverting pin relative to the inverting pin – typical.		
tdelay_min	Ibid – min		
tdelay_max	Ibid – max		

(Table 3 cont.)

Note 4: IBIS says required if [Diff Pin] used. But, 3Com says optional

Table 3 (cont.): IBIS Package and Pin Properties

Keyword	Description	Minimum Requirement	Comments
[Series Pin Mapping]	Used to associate 2 pins joined by a series model. 1 st column is the series pin for which Zinput is measured.	Optional	All pin numbers must match the numbers in the [Pin] section.
pin_2	2 nd column is the other connection. Subparameter of [Series Pin Mapping	Note 9	Differential pair termination, crossbar switching, etc., can be described.
model_name	Model connected between the series pins. Subparameter of [Series Pin Mapping].	Note 9	Normally, series switch model names are used. See table 3.
function_table_group	An alphanumeric designator string that associates sets of series switch pins that are switched together. Subparameter of [Series Pin Mapping]	Optional	Used to associate switches whose switching is synchronized by a common control function.
[Series Switch Groups]	Defines allowable switching combinations (states) of series switches using the names of the groups used in function_table_group subparameter of [Series Pin Mapping].	Optional	Each state line contains an allowable configuration. Uses names of groups found in function_table_group column above.
On	A typical state line starts with an 'On' followed by all of the on-state group names	Note 10	Subparameter of [Series Switch Groups].
Off	A typical state line starts with an 'Off' followed by all of the off-state group names	Note 10	Subparameter of [Series Switch Groups].

Note 9:

Required if [Series Pin Mapping] keyword used. This mapping covers only the series paths between pins. The package parasitics and any other elements such as additional capacitance or clamping circuitry are defined by the model_name that is referenced in the [Pin] keyword. The model_names under the [Pin] keyword that are also referenced by the [Series Pin Mapping] keyword may include any legal model or reserved model except for Series and Series_switch models.

Note 10:

Required if [Series Switch Groups] keyword used. Only one of 'On' or 'Off' is required since the undefined states are assumed to be the opposite of the explicitly defined states. The first line defines the default state of the series of switches.

Table 4: IBIS V-I Behavioral Properties

Keyword	Description	Minimum Requirement	Comments
[Model]	Begins behavioral description of one of the component's I/O cells	IBIS-Yes 3Com-Yes	
Model_type	Must be one of the following: Input, Output, I/O, 3-state, Open_drain, I/O_open_drain, Open_sink, I/O_open_sink, Open_source, I/O_open_source, Input_ECL, Output_ECL, I/O_ECL, Terminator, Series and Series_switch	IBIS-Yes 3Com-Yes	Sub parameter of [Model] Some V-I and/or V-T curves may not apply to certain I/O types. See Table 5.
C_comp	Sub parameter of [Model] - Die capacitance of the I/O cell.	IBIS-Yes 3Com-Yes	Model sub parameter. Should not include package capacitance. But, often does.
Polarity	Sub parameter of [Model]	Optional	– inverting or non-inverting
Enable	Sub parameter of [Model] –	Optional	Active High or Active Low
[Vinl]	Sub parameter of [Model] – input threshold - low limit of population (for Input & I/O)	IBIS-Yes 3Com-Yes	Used to automate flight time measurements
[Vinh]	Sub parameter of [Model] – input threshold - high limit of population (for Input & I/O)	IBIS-Yes 3Com-Yes	Used to automate flight time measurements
Vol	Used to automate flight time measurements. Not an IBIS spec.	IBIS-NA 3Com-Yes	Output low state voltage - high limit of population
Voh	Used to automate flight time measurements. Not an IBIS spec.	IBIS-NA 3Com-Yes	Output high state voltage - low limit of population
Technology	Not an IBIS spec.	IBIS-NA 3Com-Yes	Ex.: GTLP, CMOS, etc.

(Table 4 cont.)

Table 4 (cont.): IBIS V-I Behavioral Properties

Keyword	Description	Minimum Requirement	Comments
[Pulldown]	Low state driver V-I curve data.	IBIS-Yes 3Com-Yes	Note 5
[Pullup]	High state driver V-I curve data..	Note 5	V-data referenced to Vcc power supply, not ground.
[GND Clamp]	V-I curve data of ESD diode structure.	Note 5	Can be present on inputs and/or outputs.
[POWER Clamp]	V-I curve data of ESD diode structure.	Note 5	Can be present on inputs and/or outputs. V-data referenced to Vcc power supply, not ground

(Table 4 cont.)

Note 5:

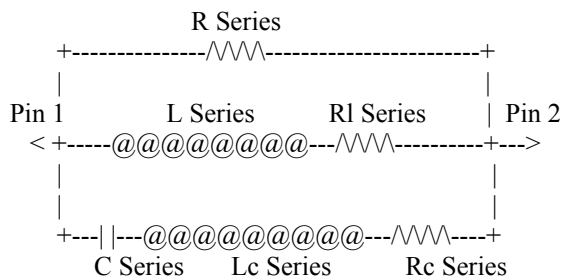
Yes, if present in device - must include at least typical data. If min & max missing they must be NA. **BY DEFINITION** measured over $-V_{cc}$ to $+2V_{cc}$ range. Referenced to ground, therefor the same as output V-I curve as in data book format.

Table 4 (cont.): IBIS V-I Behavioral Properties

Keyword	Description	Minimum Requirement	Comments
Series or Series_switch Model_types	These two new Model_type(s) in addition to "Output, Input," etc., have been added to IBIS	Note 13	The data for these keywords allow the definition of a Series or Series_switch R, L, or C path.
[On], [Off]	'On' state models are positioned under [On]. 'Off' state models are positioned under [Off].		
[R Series]	Series resistor between pins 1 & 2		
[L Series]	Series inductor between pins 1 & 2		
[C Series]	Series capacitor between pins 1 & 2		
[Rl Series]	Series resistance of inductor. Defined only if [L Series] exists		
[Rc Series]	Series resistance of capacitor. Defined only if [C Series] exists		
[Lc Series]	Series inductance of capacitor. Defined only if [C Series] exists		
[Series Current]	V-I tables for voltages measured at pin1 w.r.t. pin2		
[Series MOSFET]	V-I tables for voltages measured at pin2 for a given Vds setting.		

(Table 4 cont.)

Note 13: Only keywords associated with Series_switch electrical models are permitted under [On] or [Off]. The Series electrical models describe the path for one state only and do not use the [On] and [Off] keywords. This series RLC model is defined to allow IBIS to model simple passive models and/or parasitics. The model is:



[Rc Series] and [Lc Series] shall be defined only if [C Series] exists. [Rc Series] is 0 ohms if it is not defined in the path. [Lc Series] is 0 henries if it is not defined in the path. C_comp values are ignored for these keywords.

Table 4 (cont.): IBIS V-I Behavioral Properties

Keyword	Description	Minimum Requirement	Comments
[Pullup Reference]	Can define a voltage high rail other than Vcc bus	IBIS-Yes 3Com-Yes	Note 6. If voltage range not used.
[Pulldown Reference]	Can define a non-zero low rail (ground) bus	Note 6	
[GND Clamp Reference]	Can define a non-zero low rail (ground) bus		
[POWER Clamp Reference]	Can define a voltage high rail other than Vcc bus		
[Model Selector]	Used to pick a [Model] from a list of [Model]s for a pin that uses a programmable buffer. When used, the [Model Selector] keyword is followed by a particular model that is listed under the [Model] keyword.	Optional Note 11	The section under [Model Selector] contains 2 fields. Several pins can reference a particular [Model Selector] name.
(1 st field)	Contains the [Model] names called by the [Model Selector] name.	Note 11	
(2 nd field)	Contains a short description of the model names		

(Table 4 cont.)

Note 6:

Yes, if [Voltage Range] not used

Note 11:

IBIS 3.2 [Model Selector] rules are complex enough to be repeated here:

"Usage Rules: A programmable buffer must have an individual [Model] section for each one of its modes used in the .ibs file. The names of these [Model]s must be unique and can be listed under the [Model Selector] keyword and/or pin list. The name of the [Model Selector] keyword must match the corresponding model name listed under the [Pin] or [Series Pin Mapping] keyword and must not contain more than 20 characters. A .ibs file must contain enough [Model Selector] keywords to cover all of the model selector names specified under the [Pin] and [Series Pin Mapping] keywords. The section under the [Model Selector] keyword must have two fields. The two fields must be separated by at least one space or tab character. However, the use of tab characters is not recommended in general. The first field lists the [Model] name (up to 20 characters long). The second field contains a short description of the [Model] shown in the first field. The contents and format of this description is not standardized, however it shall be limited in length so that none of the descriptions exceed the 80-character length of the line that it started on. The purpose of the descriptions is to aid the user of the simulator tool in making intelligent buffer mode selections and it can be used by the simulator tool in a user interface dialog box as the basis of an interactive buffer selection mechanism.

The first entry under the [Model Selector] keyword shall be considered the default by the simulator tool for all those pins that call this [Model Selector]. The operation of this selection mechanism implies that a group of pins that use the same programmable buffer (i.e. model selector name) will be switched together from one [Model] to another. Therefore, if two groups of pins, for example an address bus and a data bus, use the same programmable buffer, and the user must have the capability to configure them independently, one can use two [Model Selector] keywords with unique names and the same list of [Model] keywords. However, the usage of the [Model Selector] is not limited to these examples. Many other combinations are possible."

Table 4 (cont.): IBIS V-I Behavioral Properties

Keyword	Description	Minimum Requirement	Comments
[Model Spec]	Defines 4 columns under which [Model Spec] subparameters are defined.	Optional	
Vinh	Input threshold voltage high		
Vinl	Input threshold voltage low		
Vinh-	Hysteresis threshold voltage high min V_t -		
Vinh+	Hysteresis threshold voltage high max V_t +		
Vinl-	Hysteresis threshold voltage low min V_t -		
Vinl+	Hysteresis threshold voltage low max V_t +		
S_overshoot_high	Static overshoot high voltage		
S_overshoot_low	Static overshoot low voltage		
D_overshoot_high	Dynamic overshoot high voltage		
D_overshoot_low	Dynamic overshoot low voltage		
D_overshoot_time	Dynamic overshoot time		
Pulse_high	Pulse immunity high voltage		
Pulse_low	Pulse immunity low voltage		
Pulse_time	Pulse immunity time		
Vmeas	Measurement voltage for timing measurements		

(Table 4 cont.)

Table 4 (cont.): IBIS V-I Behavioral Properties

Keyword	Description	Minimum Requirement	Comments
[Add Submodel]	Adds special functionality to an existing top level [Model] as contained in the submodel or list of submodels.	Optional	Submodel type cannot conflict with the top level model type that calls it.
[Submodel]	Defines the submodel with a set of keywords and subparameters used for the [Model] along with other parameters defined below.		C_comp is not permitted under the [Submodel] keyword. Note 14
Mode	Submodel modes are "Driving," "Non-Driving" or "All."	Note 14	
Submodel_type	The only permitted types are Dynamic_Clamp and Bus_Hold	Note 14	
	Dynamic_Clamp		Subparameter of Submodel_type
	Bus_Hold		
[Submodel Spec]	Defines 4 columns under which data and information sub parameters are defined for submodels	Optional	
V_trigger_r	Rising edge trigger voltage		Subparameter of [Submodel Spec]
V_trigger_f	Falling edge trigger voltage		
Off_delay	Turn-off delay from V_trigger_r or V_trigger_f		
[GND Pulse Table]	Used to spec the offset voltage Vs time of [GND Clamp] tables within submodels.	Optional	
[POWER Pulse Table]	Used to spec the offset voltage Vs time of [POWER Clamp] tables within submodels.	Optional	

(Table 4 cont.)

Note 14:

Required if [Submodel] is used. Keywords Pullup, Pulldown, GND Clamp, POWER Clamp, Ramp, Rising Waveform & Falling Waveform are permitted. Keywords Pullup Reference, Pulldown Reference, GND Clamp Reference, POWER Clamp Reference, are not permitted. The voltage settings are inherited from the top-level model.

Table 4 (cont.): IBIS V-I Behavioral Properties

Keyword	Description	Minimum Requirement	Comments
[TTgnd]	Transit time parameter for a [GND Clamp]	Optional Note 15	Used to estimate transit time capacitance for GND Clamp
[TTpower]	Transit time parameter for a [POWER Clamp]		Used to estimate transit time capacitance for POWER Clamp
TT(typ)	Subparameters of TTgnd and TTpower.		
TT(min), TT(max)	Subparameters of TTgnd and TTpower.		

Note 15

The transit time capacitance is added to C_comp. It is in a Spice reference model as $C_t = TT * d(I_d)/d(V_d)$ where $d(I_d)/d(V_d)$ defines the DC conductance at the incremental DC operating point of the diode, and TT is the transit time. This expression does not include any internal series resistance. Such a resistance is assumed to be negligible in practice.

Assume that the internal diode current (I_d) - voltage (V_d) relationship is $I_d = I_s * (\exp(q(V_d)/kT) - 1)$ where I_s is the saturation current, q is electron charge, k is Boltzmann's constant, and T is temperature in degrees Kelvin. Then $d(I_d)/d(V_d)$ is approximately $(q/kT) * I_d$ when the diode is conducting, and zero otherwise. This yields the simplification $C_t = TT * (q/kT) * I_d$. The I_d is found from the [GND Clamp] and [POWER Clamp] operating points, and the corresponding TTgnd or TTpower is used to calculate the C_t value. If the [Temperature Range] keyword is not defined, then use the default "typ" temperature for all C_t calculations. The effective TT parameter values are intended to APPROXIMATE the effects. They may be different from the values found in the Spice diode equations. Refer to the NOTES ON DATA DERIVATION METHOD for extracting the effective values.

Table 5: IBIS V-T Behavioral Properties

Keyword	Description	IBIS Requirement	Comments
[Ramp]	Slew Rate of Driver, i.e., output. IBIS format is data columns left to right - typ-min-max – usually leading to confusion. Includes effect of C_comp	IBIS-Yes 3Com-Yes	Note 19
dV/dt_r	Rise Slew: measured with R_load to Vcc when driving high.	Yes	Sub parameter of [Ramp]
dV/dt_f	Fall Slew: measured with R_load to GND when driving low.		
R_load	Test load for measuring [Ramp] parameters.	Yes, if not 50 Ω	
Vmeas	When switching data supplied, buffer delay can be recalculated for different loading and can be subtracted from total delay to get wire delay for Timing simulators.	Optional	Testload: See Figure 2 below
Cref			Ibid
Rref			Ibid – same as R_load?
Vref			Ibid

(Table 5 cont.)

Note 19:

– **BY DEFINITION** – Measured over 20% to 80% of full 0% - 100% swing of output. 20%-80% range set to avoid non-linearities (ambiguities) made worse by –Vcc to +2Vcc range.

Table 5 (cont.): IBIS V-T Behavioral Properties

Keyword	Description	IBIS Requirement	Comments
[Rising Waveform]	V-T curve data of rising edge. Supersedes dV/dt_r when present. Will be measured over 0% -100% of the output swing.	Optional - Note 8	Much better than [Ramp] data because non-linearity detail provided
[Falling Waveform]	V-T curve data of falling edge. Supersedes dV/dt_f when present. Will be measured over 0% -100% of the output swing.		
R_fixture	Test fixture data for measuring [Rising/ Falling Waveform]	IBIS-Yes 3Com-Yes	See Figure 3
C_fixture, L_fixture		Optional	
V_fixture		IBIS-Yes 3Com-Yes	
V_fixture_min, V_fixture_max		Optional	
R_dut, C_dut, L_dut,			

(Table 5 cont.)

Note 8:

Inclusion of V-T curves rather than just simple slew rate / ramp rate data is becoming more common. In lower frequency and simple topologies (point-point for example) V-T curves don't add a lot of accuracy. But, in topologies that tend towards a lot of high frequency reflections (multidrop busses with significant stub lengths) they can be a key differentiation in getting an accurate simulation. This is particularly seen in bus drivers that have been designed to avoid such reflections by having "soft" turnon and turnoff (example GTLP). The behavior of such devices in complex topologies simply cannot be modeled by simple slew rate information.

Table 5 (cont.): IBIS V-T Behavioral Properties

Keyword	Description	Minimum Requirement	Comments
[Driver Schedule]	A 5 column table that describes the relative model switching sequence and hierarchy for referenced models to produce a multi-staged driver.	Optional	Note 18. The Driver Schedule keyword is placed under V-T characteristics because of its direct impact on those behaviors.
Rise_on_dly	Beginning of the low-to-high transition. Referenced to time 0.		
Rise_off_dly	End of the low-to-high transition. Referenced to time 0		
Fall_on_dly	Beginning of the high-to-low transition. Referenced to time 0		
Fall_off_dly	End of the high-to-low transition. Referenced to time 0		

Note 18:

For each model the transition sequence must be complete: i.e., it must start and end at the same state. Use 'NA' when no transition is applicable.

Only the [Pulldown] and [Pullup] tables and transition data [Ramp] or [Rising Waveform] and [Falling Waveform] data are used from each model that is referenced. The [Model] keyword provides the specification information, [GND Clamp] and [POWER Clamp], and C_comp, regardless of information contained in the referenced models.

The added models typically consist of Open_sink (Open_drain) or Open_source models to provide sequentially increased drive strengths. The added drive may be removed within the same transition for a momentary boost or during the opposite transition. The syntax also allows for reducing the drive strength.

Note that the Rise_on_dly, Rise_off_dly, Fall_on_dly, Fall_off_dly parameters are single value parameters, so typical, minimum and maximum conditions cannot be described with them directly. In order to account for those effects, one can refer to the fastest waveform table with the delay number and then insert an appropriate amount of horizontal lead in section in those waveforms, which need more delay.

Note: In a future release, the [Driver Schedule] keyword may be replaced by a newer method of specification that is consistent with some other planned extensions. However, the [Driver Schedule] syntax will continue to be supported.

Table 6: IBIS Electrical Board Description

Keyword	Description	Minimum Requirement	Comments
[Begin Board Description]	Describes a "board level component," or substrate, which can connect to another board through a set of user visible pins.	Optional Note 16	Can contain components or even other boards
[Manufacturer]	Maker of the component	IBIS-Yes 3Com-Yes	
[Number of Pins]	Tells the parser the number of externally accessible electrical connection pins to expect.	IBIS-Yes 3Com-Yes	
[Pin List]	Tells the parser the pin names and the signal_names associated with them.	IBIS-Yes 3Com-Yes	Pins can be specified with POWER, GND or NC (no connect)
Signal_name	Sub parameter of [Pin List]	IBIS-Yes 3Com-Opt	
[End Board Description]	End of the electrical interconnect description	IBIS-Yes 3Com-Yes	
[End]	Defines the end of the .ibs, .pkg or .ebd file	IBIS-Yes 3Com-Yes	

(Table 6 cont.)

Note 16:

An electrical board description file (a .ebd file) is defined to describe the connections of a board level component. A .ebd file is intended to be a stand-alone file, not associated with any .ibs file.

A fundamental assumption regarding the electrical board description is that the inductance and capacitance parameters listed in the file are derived with respect to well-defined reference plane(s) within the board. Also, this current description does not allow one to describe electrical (inductive or capacitive) coupling between paths. It is recommended that if coupling is an issue, then an electrical description be extracted from the physical parameters of the board. What is, and is not, included in an Electrical Board Description is defined by its boundaries. For the definition of the boundaries, see the Description section under the [Path Description] Keyword.

For example, a SIMM module is a board level component that is used to attach several DRAM components on the PCB to another board through edge connector pins. An electrical board description file (a .ebd file) is defined to describe the connections of a board level component between the board pins and its components on the board.

Table 6 (cont.): IBIS Electrical Board Description

Keyword	Description	Minimum Requirement	Comments
[Path Description]	Describes the connections between the external pins and other pins on the board such as interface ICs.	Yes	Note 21
Len	Physical length of a section	Note 20	Given in terms of arbitrary units.
L	Series inductance of a section		Given in terms of "inductance/unit length"
R	Series resistance of a section		Ibid
C	Series capacitance of a section		ibid
Fork	Indicates that the sections following, and up to Endfork, are part of a branch off the main package stub.		
Endfork	End of the fork, or branch.		Each Fork must have a corresponding Endfork
Node	reference_designator.pin. Used when the connection path hooks up to the pin of another, externally defined component.		
Pin	Marks the point at which a path description connects to a user accessible pin.		
[Reference Designator Map]	Maps a reference designator to a component or electrical board description contained in an .ibs or .ebd file.	Note 17	Lists all the reference _designators called out by the Node sub parameters used in the path descriptions

Note 17:

Required if Node is used. The [Reference Designator Map] keyword must be followed by a list of all of the reference designators called out by the Node subparameters used in the various path descriptions. Each reference designator is followed by the name of the .ibs or .ebd file containing the electrical description of the component or board, then the name of the component itself as given by the .ibs or .ebd file's [Component] or [Begin Board Description] keyword respectively. By default the .ibs or .ebd files are assumed to exist in the same directory as the calling .ebd file. It is legal for a reference designator to point to a component that is contained in the calling .ebd file.

Note 20:

Subparameter of [Path Description]: The Len, L, R, and C subparameters specify the length, the series inductance, resistance, and the capacitance to ground of each section in a path description.

Len, or length is in an integer number of "units." For example, if the length of the section is 2 'units' and the inductance is 1.5 nh / unit, then the inductance of the section is 3.0 nh. If a Len of zero is specified then the L/R/C values are the total for the section. If $Len \neq 0$, then the total L/R/C for that section is multiplied by that value.

The Fork and Endfork subparameters denote branches from the main pin-to-node or pin-to-pin connection path. The Node subparameter is used to reference the pin of a component or board as defined in a .ibs or .ebd file. The Pin subparameter is used to indicate the point at which a path connects to a user visible pin. The Fork subparameter indicates that the sections following (up to the Endfork subparameter) are part of a branch off of the main connection path. This subparameter has no arguments. Endfork subparameter indicates the end point of a branch.

Note 21:

This keyword allows the user to describe the connection between the user accessible pins of a board level component and other pins or pins of the ICs mounted on that board. Each pin to node connection is divided into one or more cascaded "sections", where each section is described in terms of its L/R/C per unit length. The Fork and Endfork subparameters allow the path to branch to multiple nodes, or another pin. A path description is required for each pin whose signal name is not "GND", "POWER" or "NC".

Board Description and IC Boundaries:

In any system, each board level component interfaces with another board level component at some boundary. Every electrical board description must contain the components necessary to represent the behavior of the board level component being described within its boundaries. The boundary definition depends upon the board level component being described.

For CARD EDGE CONNECTIONS such as a SIMM or a PC Daughter Card plugged into a SIMM Socket or Edge Connector, the boundary should be at the end of the board card edge pads as they emerge from the connector.

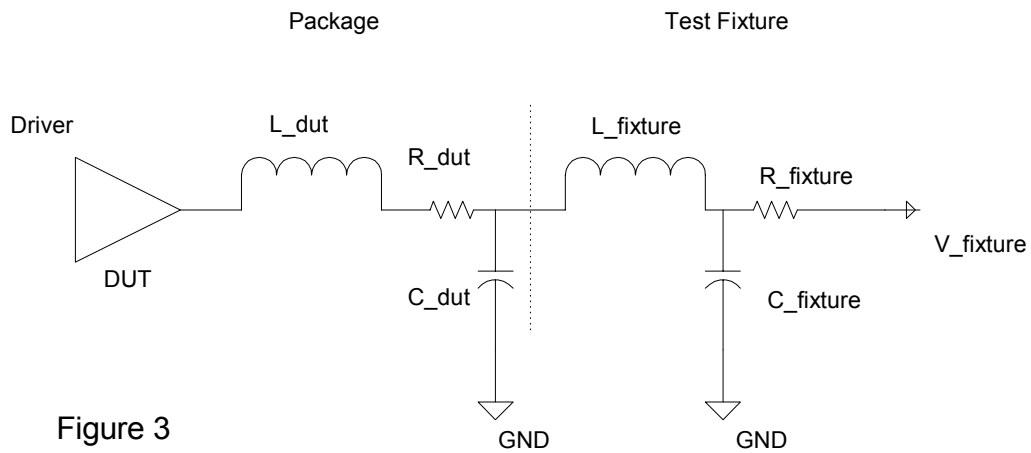
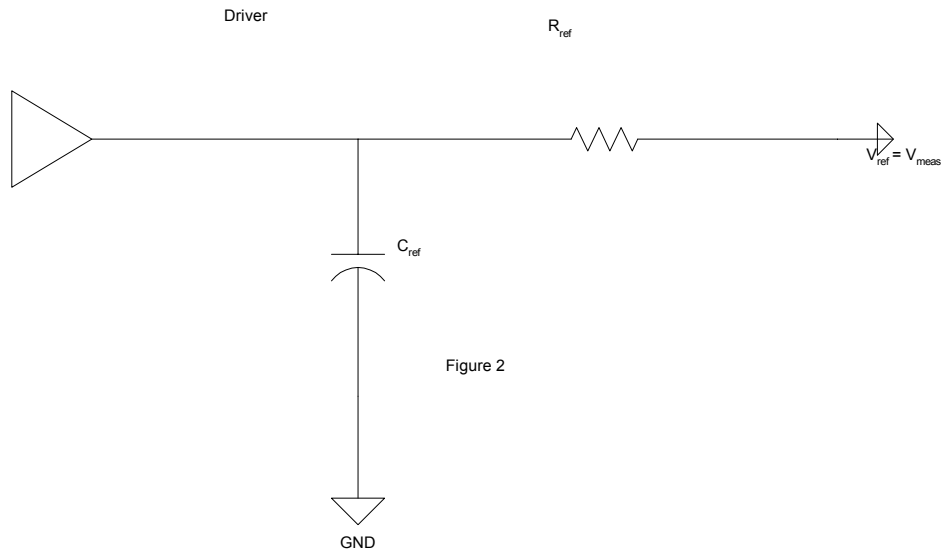
For any THROUGH-HOLE MOUNTED COMPONENT, the boundary will be at the surface of the board on which the component is mounted.

SURFACE MOUNTED COMPONENT models end at the outboard end of their recommended surface mount pads.

If the board level component contains an UNMATED CONNECTOR, the unmated connector will be described in a separate file, with its boundaries being as described above for the through-hole or surface mounted component.

Each individual connection path (user pin to node(s)) description begins with the [Path Description] keyword and a path name, followed by the subparameters used to describe the path topology and the electrical characteristics of each section of the path. Each occurrence of the [Path Description] keyword must be followed by a unique path name. Every signal pin (pins other than POWER, GND or NC) must appear in one and only one path description per [Begin Board Description]/[End Board Description] pair. Pin names do not have to appear in the same order as listed in the [Pin List] table. The individual subparameters are broken up into those that describe the electrical properties of a section, and those that describe the topology of a path.

Test Fixtures Used in Above:



5.2 Requirements by Model Type

Behavior information that changes by model type in the device (and in the IBIS spec) is the presence/absence and relevance of the V-I and V-T curves and switching threshold data. “Yes” in the table below indicates a model requirement with the qualifier “when the feature is present in the device.” V-T data requirements are the same as those for pullup and pulldown curves. That is, when those structures are present in the device then V-T data is required. In the case of open pullups and open pulldowns the data is still required. In those cases the method of data generation is to use the same test fixture/circuit that the semiconductor supplier uses for specifying delay times.

Table 7: V-I Curves and Threshold Voltages by Model & Technology

Model Type	Pull Up	Pull Down	Ground Clamp	Power Clamp	Thresholds
Input			Yes	Yes	Vinl, Vinh
Output	Yes	Yes	Yes	Yes	Vol, Voh
I/O	Yes	Yes	Yes	Yes	Vinl, Vinh, Vol, Voh
3-State	Yes	Yes	Yes	Yes	Vol, Voh
Open_drain		Yes			Vol, Voh
Open_sink		Yes			Vol, Voh
I/O_open_sink		Yes	Yes	Yes	Vinl, Vinh, Vol, Voh
Open_source	Yes			Yes	Vol, Voh
I/O_open_source	Yes		Yes	Yes	Vinl, Vinh, Vol, Voh
Input_ECL					Vinl, Vinh
Output_ECL	Yes	Yes			Vol, Voh
I/O_ECL	Yes	Yes			Vinl, Vinh, Vol, Voh
Terminator					None
Series	Described by Series or Series_switch Model_types				
Series_switch	Described by Series or Series_switch Model_types				

5.3 3Com Standard Vs Add-On Requirements

Definitions:

The “Standard Model” is based on what is required to construct an IBIS file that will function to 3 COM’s minimum standards. The “Add-On” model elements are the remaining IBIS v2.1 model elements that can add to the effectiveness and accuracy of signal integrity analysis in the judgement of the design engineer. He/she adds the elements of their choice to the request for an IBIS model.

Guidelines for forming the design choices of which add-on elements to request are found in “How to Use the IBIS Model.”

IBIS Model

Standard

Add-On

General Properties:

IBIS Ver., File Name, File Rev, Date,
Source, Copyright, Manufacturer,

General Properties:

Comment Char (new), Notes, Disclaimer

Component Properties:

Component, Voltage Range, Temperature
Range

Component Properties:

Si_location, Timing_location

Package and Pin Properties:

Package, Pin⁽²⁾, Rac⁽³⁾, Cac⁽³⁾, Rgnd⁽³⁾,
Rpower⁽³⁾, Diff Pin (inv_pin)⁽³⁾⁽⁴⁾

Package and Pin Properties:

Rpin-Cpin-Lpin⁽²⁾, Signal_name, Package
Model (Define Package Model, Manufacturer,
OEM, Description, Number of Pins, Pin
Numbers, Model Data, R-L-C Matrices, Row,
Bandwidth, End Model Data), Pin Mapping
(Pulldown_ref, etc., all sub parameters as
applicable), vdiff & tdelay (all)⁽⁴⁾, Number of
Sections, Series Pin Mapping, Series Switch
Groups

Model (V-I behavioral) Properties:

Model, Model_type, Polarity, Vinl⁽³⁾,
Vinh⁽³⁾, Vol⁽³⁾, Voh⁽³⁾, C_comp, Vref,
Vmeas, Rref, Cref, Technology, Pullup⁽³⁾,
Pulldown⁽³⁾, POWER Clamp⁽³⁾, GND
Clamp⁽³⁾, Model Selector

Model (behavioral) Properties:

Enable, Pullup Reference, Pulldown Reference,
POWER Clamp Reference, GND Clamp
Reference, Model Spec, Add Submodel,
Submodel Spec, GND & POWER Pulse Table,
TTgnd, TTpower

Model (V-T behavioral) Properties:

Ramp⁽³⁾, dV/dt_r⁽³⁾, dV/dt_f⁽³⁾, R_load⁽³⁾,
Driver Schedule

Model (V-T behavioral) Properties:

Rising Waveform, Falling Waveform, R-L-
C_fixture, R-L-C_dut, V_fixture (all)

Notes:

- (2) Individual Model_type information by pin is required. But, individual pin parasitics are an add-on.
- (3) As present in the device.
- (4) Differential pair inputs or outputs must be identified by naming the inverse pin. But, launch delay and offset parameters are an add-on.

6. IBIS Model Creation

This section provides techniques by which a new IBIS model is created from scratch.

6.1. Getting Help

IBIS is an emerging standard. The current released version is 2.1 with 3.1 due out sometime around the beginning of 1999. As well, there is an “IBIS Accuracy Specification” being worked on by the committee.

The IBIS Open Forum meets every 3 weeks via teleconferencing and e-mail and occasionally in person to ratify changes and set future directions. Most activities are handled via the email reflector at:

ibis@vhdl.org

To add your name, send your email address to:

ibis-request@vhdl.org

To suggest changes and improvements, submit a “BIRD (Buffer Issue Resolution Document)” to this email address.

You can check the latest released version of the IBIS spec at:

IBIS directory of publications:

<http://www.eda.org/pub/ibis>

ANSI/EIA-656 IBIS Home Page:

<http://www.eia.org/eig/ibis/ibis.htm>

Additional help can be found at:

ERL IBIS Project:

http://www2.ncsu.edu/eos/project/erl_html/erl_ibis.htm

IBIS Cookbook:

http://www2.ncsu.edu/eos/project/erl_html/ibis/cookbk_ToC.htm

ERL Software:

http://www2.ncsu.edu/eos/project/erl_html/erl_software.htm

The use of an “IBIS Golden Parser” software program to check syntax during the preparation of an IBIS model file will be standard for 3Com. These rules are scattered throughout the text of the IBIS spec and are tedious to find, memorize and keep track of. The IBIS “**Golden Parser**” - current, past and future versions, are downloadable free from:

ANSI/EIA-656 IBIS – Tools:

<http://www.eia.org/eig/ibis/tools.html>

6.2. Model Properties by Technology Type

Refer to Table 5 above for a listing of model properties by technology type.

6.3 Package Properties

Package properties include a couple of levels of sophistication in IBIS depending on how detailed you want to get. This in keeping with the intent of the IBIS committee that:

- A given die (I/O model V-I and V-T curves) can be modeled in different packages
- Parasitic model detail and sophistication should be driven by design needs

At the minimum required level you will have the package and pin properties. Package allows you to assign a common value of R, L and C parasitics to all pins in the package. Pin allows you to assign the various model types (model_name) and signal names to each pin.

The next level of details are the specific R, L and C pin parasitics associated with individual pins. Individually assigned R, L and C pin parasitics override the package assigned R, L and C pin parasitics.

The next level of complexity, [Package Model], can be a file on its own with a .pkg extension. Else, the Package Model keyword can be included in the IBIS file. This level of detail includes manufacturer of the die, manufacturer of the package, package description, number of pins and pin numbers and R [Resistance Matrix], L [Inductance Matrix], and C [Capacitance Matrix] parasitic matrices. When present the R, L and C parasitic matrices override the R, L and C parasitics assigned to individual pins and the global package R, L and C.

At this first level of increased detail the assumption might be that there is no mutual parasitics between pins, only self-parasitics. But, then the Package Model keyword would be hardly worth the bother. Most of the time when Package Model is used it's because mutual pin coupling is being modeled. Some simulators have adapted the IBIS package model to also handle connectors and cable bundles. Packages with up to 1000 pins have been modeled this way. IBIS has incorporated keywords for banded, sparse and full matrices to help limit complexity in larger pin count packages.

IBIS 3.2 has added constructs for forks and sections to the means of modeling interconnect. Forks allow branching. Sections split up a length of interconnect and allow it to be modeled as a distributed network. These models can be considered "in addition to" RLC matrices. But, if "combined with" the RLC matrix each section would have its own RLC matrix (including mutual coupling parasitics) in cascade with the other sections. This allows for modeling items like connectors as distributed structures.

Also, for more sophisticated package modeling IBIS provides a means of associating individual I/O cell pins with particular power and ground pins (busses). The [Pin Mapping] keyword and its pulldown_ref, pullup_ref, gnd_clamp_ref and power_clamp_ref allow you to associate the I/O cells.

Keywords of Pulldown Reference, Pullup Reference, GND Clamp Reference and Power Clamp Reference allow you individually name and reference the several busses. With these keywords voltages can be set individually on busses.

6.4. V-I Curve Properties

V-I curve properties include data tables of current Vs voltage. They are found under the Pullup, Pulldown, GND Clamp and Power Clamp keywords. As with all IBIS data, Typical values are required, Min and Max are optional. In an ASCII format this has lead to the left-to-right formatting of Typ-Min-Max, a constant source of misinterpretation. As well, the Pullup and Power Clamp I/O pin voltages are referenced to their supply voltage, not ground as found on data sheets.

V-I curves are measured over a range of $-V_{cc}$ to $+2V_{cc}$ by definition and in response to the fact that reflections can set up that range worst case.

6.5. Ground and Power Bounce Properties

The Pin Mapping keyword and its properties of pulldown_ref, etc., along with the pin R, L and C properties of the power and ground pins tell the simulator what the package contributions to ground and power bounce will be.

6.6. Differential Pair Properties

Differential pair properties include [Diff Pin] for associating the 2 pins and inv_pin for naming which one is the inverting pin. Threshold voltage offset between the two can be specified with vdiff and launch delay offset can be specified with tdelay_typ (_min, _max).

6.7. V-T Curve Properties

V-T properties include a couple of levels of sophistication in IBIS depending on how accurate you want to get. The [Ramp] keyword and its properties of dV/dt_r and dV/dt_f give you the basic slew, or edge, rate information. This is the least costly to generate off of a switching waveform. The IBIS convention for rise and fall time is to measure it from 20 % to 80 % of the output 0 to V_{cc} swing. The assumption is that there is minimal ringing and that R_{load} is 50 ohms unless otherwise specified. The 20 % to 80 % range is to stay on the most linear portion of the waveform.

It is important to remember that the usual (traditional) data sheet definition of rise/fall time is taken over a 10 % to 90 % range and to make the necessary translation.

The rise and fall time are chiefly affected by the loading on the output buffer and its ability to switch on/off and charge/discharge its output (die – C_{comp}) capacitance. All V-T curves include the effect of C_{comp} since there is no way to isolate out its effects in real life. However, the effects of external loading can be adjusted for if the test fixture information for measuring the original V-T waveforms is included.

The frequency content of a given output driver waveform in a given high speed digital topology is the chief determinant of the reflections that are set up. Edge rate is the most sensitive chunk of this. But, not all edge rates are equal. Ramp rate control and smooth rounding of a driver output wave as it comes out of or into its rail voltages can easily determine if a part/circuit will work or not.

Therefore, the next level of sophistication in IBIS is to include the actual V-T data points of the [Rising Waveform] and [Falling Waveform]. When present, these waveforms supercede the dV/dt_r and dV/dt_f data. As well, the test fixture information – $R_{fixture}$, $C_{fixture}$, $L_{fixture}$, $V_{fixture}$, R_{dut} , C_{dut} , and L_{dut} - is usually included when the waveforms are included.

IBIS 3.2 adds the ability to model variable drive strength outputs with [Driver Schedule]. This allows additional output cells to get turned on or off as a driver gets turned on or off. This clearly is tied into the V-T behavior of the part.

6.8. IBIS Model Data Sources: Summary Tables

Table 8: General Properties - refer to Table 1 for req./not req. definitions, etc.

Keyword	Sub Parameter	Most Likely Source	Alternate Source	Notes
[IBIS Ver]		IBIS 3.2		
[Comment Char]		IBIS 3.2	Originator can set	
[File Name]		Originator		
[File Rev]		Originator		
[Date]		Originator		
[Source]		Name of originator		
[Notes]		Originator		Optional
[Copyright]		Originator		Optional
[Disclaimer]		Originator		Optional

Table 9: Component Properties - refer to Table 2 for req./not req. definitions, etc

Keyword	Sub Parameter	Most Likely Source	Alternate Source	Notes
[Component]	Si_location Timing_location	Datasheet		
		Originator		
		Originator		
[Manufacturer]		Datasheet		
[Voltage Range]		Datasheet	Manufacturer	
[Temperature Range]		Datasheet	Manufacturer	

Table 10 (cont.): Package & Pin Properties - refer to Table 3 for req./not req. etc.

Keyword	Sub Parameter	Most Likely Source	Alternate Source	Notes
[Package]	Rpkg, Lpkg, Cpkg	Datasheet	Originator	
[Pin]	signal_name, model_name, Rpin, Lpin, Cpin	Datasheet, Manufacturer	Field solver, network analyzer	
[Package Model]		Manufacturer		
[Define Package Model]				1
[Manufacturer]		Manufacturer		2
[OEM]		Manufacturer		
[Description]		Originator		Optional
[Number of Pins]		Datasheet		
[Pin Numbers]		Datasheet		
[Number Of Sections]	Len, L, R, C, Fork, Endfork	Originator		Optional
[Model Data]				1
[Resistance Matrix]	Banded_matrix, Sparse_matrix, Full_matrix	Manufacturer	Field solver, network analyzer	
[Inductance Matrix]	Ibid	Ibid	Ibid	
[Capacitance Matrix]	Ibid	Ibid	ibid	
[Row]		Originator		3
[Bandwidth]		Originator		4
[End Model Data]		Originator		1

(Table 10 cont.)

Table 10 (cont.): Package & Pin Properties - refer to Table 3 for req./not req. etc.

Keyword	Sub Parameter	Most Likely Source	Alternate Source	Notes
[Pin Mapping]	pulldown_ref, pullup_ref, gnd_clamp_ref, power_clamp_ref	Datasheet	Manufacturer	
[Rac]		Datasheet	Manufacturer	
[Cac]		Datasheet	Manufacturer	
[Rgnd]		Datasheet	Manufacturer	5
[Rpower]		Datasheet	Manufacturer	5
[Diff Pin]	inv_pin, vdiff, tdelay_typ, tdelay_min, tdelay_max	Datasheet	Manufacturer	
[Series Pin Mapping]	pin_2, model _name, function table_group	Originator		Optional
[Series Switch Groups]	On, Off	Originator		Optional

Table 11: V-I Behavioral Properties - refer to Table 4 for req./not req., etc.

Keyword	Sub Parameter	Most Likely Source	Alternate Source	Notes
[Model]	Polarity, Enable, Vinl, Vinh, C_comp, Vref, Vmeas, Rref, Cref Model_type(s): Input, Output, I/O, 3-State, Open drain, Open_sink, I/O_open_sink, Open_source, I/O_open_source, Input_ECL, Output_ECL, I/O_ECL, Terminator, Series or Series_switch	Datasheet	Manufacturer	See figure 2
[On]		Originator	Datasheet	Optional
[Off]		Originator	Datasheet	Optional
[R Series]		Originator	Datasheet	Optional
[L Series]		Originator	Datasheet	Optional
[C Series]		Originator	Datasheet	Optional
[Rl Series]		Originator	Datasheet	Optional
[Rc Series]		Originator	Datasheet	Optional
[Lc Series]		Originator	Datasheet	Optional
[Series Current]		Originator	Datasheet	Optional
[Series MOSFET]		Originator	Datasheet	Optional

(Table 11 cont.)

Table 11 (cont.): V-I Behavioral Properties - refer to Table 4 for req./not req., etc.

Keyword	Sub Parameter	Most Likely Source	Alternate Source	Notes
3Com Requirement	Vol, Voh	Datasheet	Manufacturer	
3Com Requirement	Technology	Datasheet	Manufacturer	
[Pullup]		Datasheet, Manufacturer	SPICE simulation, measurement	
[Pulldown]		Datasheet, Manufacturer	SPICE simulation, measurement	
[GND Clamp]		Datasheet, Manufacturer	SPICE simulation, measurement	
[POWER Clamp]		Datasheet, Manufacturer	SPICE simulation, measurement	
[Pullup Reference]		Datasheet	Manufacturer	
[Pulldown Reference]		Datasheet	Manufacturer	
[GND Clamp Reference]		Datasheet	Manufacturer	
[POWER Clamp Reference]		Datasheet	Manufacturer	
[Model Selector]		Originator	Datasheet	Optional
[Model Spec]	Vinh, Vinl, Vinh-, Vinh+, Vinl-, Vinl+, S_overshoot_high, S_overshoot_low, D_overshoot_high, D_overshoot_low, D_overshoot_time, Pulse_high, Pulse low, Pulse_time, Vmeas	Datasheet	Originator	Optional

(Table 11 cont.)

Table 11 (cont.): V-I Behavioral Properties - refer to Table 4 for req./not req., etc.

Keyword	Sub Parameter	Most Likely Source	Alternate Source	Notes
[Add Submodel]	Mode (Driving, Non_Driving, All)	Datasheet	Originator	Optional
[Submodel]	Submodel_type (Dynamic_Clamp, Bus_Hold)	Datasheet	Originator	Optional
[Submodel Spec]	V_trigger_r, V_trigger_f, Off_delay	Datasheet	Originator	Optional
[GND Pulse Table]		Originator	Datasheet	Optional
[POWER Pulse Table]		Originator	Datasheet	Optional
[TTgnd]	TT(typ), TT(min), TT(max)	Datasheet	Originator	Optional
[TTpower]	ibid	Datasheet	Originator	Optional

Table 12: V-T Behavioral Properties - refer to Table 5

Keyword	Sub Parameter	Most Likely Source	Alternate Source	Notes
[Ramp]	dV/dt_r, dV/dt_f, R_load	Datasheet, Manufacturer	SPICE simulation, measurement	
[Rising Waveform]	R_fixture, R_dut, C_fixture, C_dut, L_fixture, L_dut, V_fixture, V_fixture_min, V_fixture_max	SPICE simulation, measurement	Datasheet, Manufacturer	See figure 3
[Falling Waveform]	Ibid	Ibid	Ibid	
[Driver Schedule]	Rise_on_dly, Rise_off_dly, Fall_on_dly, Fall_off_dly	Datasheet	Originator	Optional

Table 13: IBIS Board Description Properties - refer to Table 6 for req./not req., etc.

Keyword	Sub Parameter	Most Likely Source	Alternate Source	Notes
[Begin Board Description]		Originator		
[Manufacturer]		Datasheet		
[Number of Pins]		Datasheet		
[Pin List]	Signal_name	Originator	Datasheet	
[Path Description]	Len, R, L, C, Fork, Endfork, Node, Pin	Originator		
[Reference Designator Map]				
[End Board Description]		Originator		
[End]		originator		

7. IBIS Model Data Generation Methods

7.1. General Remarks on Data Derivation

Generating a complete IBIS file for a large IC can be a lot of work. Consider consulting with the end user to find out if some pins are not going to be simulated and can be ignored or given a default model. For example, static control pins rarely get simulated.

Determine how many unique buffer designs and how many package types are to be tried in the part to be modeled. Each unique buffer and package combination requires a different model. Find out if the device will be used in a mixed power supply environment. For example, the ESD diodes may be referenced to a different supply than the buffers.

The required "typ" column for all data represents typical operating conditions. For most [Model] keyword data, the "min" column describes slow, weak performance, and the "max" column describes the fast, strong performance. You can use slow, weak components or models to or fast, strong components or models to derive the data in the min and max columns under the corresponding voltage and temperature derating conditions for these columns. You can also use typical components or models derated by voltage and temperature and apply proprietary "X%" and "Y%" factors described later for further derating. This methodology has the nice feature that the data can be derived either from semiconductor vendor proprietary models, or typical component measurement over temperature/voltage.

Temperature range contains the temperature, which amplifies the slow, weak conditions in the "min" column, and the temperature, which amplifies the fast, strong conditions in the "max" column. Therefore, the "min" column for [Temperature Range] will contain the lowest temperature for bipolar models (TTL and ECL) but, the highest value for CMOS models. The "min" and "max" columns for all remaining keywords and subparameters contains the smallest and largest magnitude values

C_comp is considered an independent variable. This is because C_comp includes bonding pad capacitance, which does not necessarily track fabrication process variations. The conservative approach to using IBIS data associates large C_comp values with slow, weak models, and small C_comp values with fast, strong models."

Default temperatures under which all V/I tables are extracted are given below. The same defaults also are stated for the [Ramp] subparameters, but they also apply for the waveform keywords. The stated voltage ranges for V/I tables cover the most common, single supply cases. When multiple supplies are specified, the voltages extend similarly to values that reflect reflection coefficients of +1 to -1 in reflected wave simulations.

For the [Ramp] subparameters, the default test load and voltages are provided. However, the test load can be entered directly by the R_load subparameter. The allowable test loads and voltages for the waveform keywords are stated by required and optional subparameters; no defaults are needed. Even with waveform keywords, the [Ramp] keyword continues to be required so that the IBIS model remains operational in situations, which do not support waveform processing.

The following discussion lists test details and default conditions.

1) V/I tables for CMOS models:

typ = typical voltage, typical temp Deg C, typical process

min = minimum voltage, max temp deg C, typical process, minus "X%"

max = maximum voltage, min temp deg C, typical process, plus "X%"

V/I tables for bipolar models:

typ = typical voltage, typical temp deg C, typical process

min = minimum voltage, min temp deg C, typical process, minus "X%"

max = maximum voltage, max temp deg C, typical process, plus "X%"

The semiconductor vendor specifies nominal, min, and max temperature. The default range is 50 deg C nom, 0 deg C min, and 100 deg C max temperatures.

X% and Y% should be statistically determined by the semiconductor vendor based on numerous fab lots, test chips, process controls, etc.. The value of X need not be published in the IBIS file, and may decrease over time as data on the I/O buffers and silicon process increases.

Temperatures are junction temperatures.

2) Voltage Ranges:

Points for each table must span the voltages listed below:

Table	Low Voltage	High Voltage
-----	-----	-----
[Pulldown]	GND - POWER	POWER + POWER
[Pullup]	GND - POWER	POWER + POWER
[GND Clamp]	GND - POWER	GND + POWER
[POWER Clamp]	POWER	POWER + POWER
[Series Current]	GND - POWER	GND + POWER
[Series MOSFET]	GND	GND + POWER

As described in the [Pulldown Reference] keyword section, the V/I tables of the [Pullup] and the [POWER Clamp] structures are 'Vcc relative', using the equation:

$$V_{table} = V_{cc} - V_{output}$$

When tabulating output data for ECL type models, the voltage points must span the range of Vcc to Vcc - 2.2 V. This range applies to both the [Pullup] and [Pulldown] tables. Note that this range applies ONLY when characterizing an ECL output.

These voltage ranges must be spanned by the IBIS data. Data derived from lab measurements may not be able to span these ranges as such and so may need to be extrapolated to cover the full range. This data must not be left for the simulator to provide.

3) Ramp Rates:

The following steps assume that the default load resistance of 50 ohms is used. There may be models that will not drive a load of only 50 ohms into any useful level of dynamics. In these cases, use the semiconductor vendor's suggested (nonreactive) load and add the load subparameter to the [Ramp] specification.

The ramp rate does not include packaging but does include the effects of the C_comp parameter; it is the intrinsic output stage rise and fall time only. The ramp rates (listed in AC characteristics below) should be derived as follows:

a. If starting with the silicon model, remove all packaging. If starting with a packaged model, perform the measurements as outlined below. Then use whatever techniques are appropriate to derive the actual, unloaded rise and fall times.

b.
If: The Model_type is one of the following: Output, I/O, or 3-state (not open or ECL types); Then: Attach a 50 ohm resistor to GND to derive the rising edge ramp. Attach a 50 ohm resistor to POWER to derive the falling edge ramp.

If: The Model_type is Output_ECL, I/O_ECL, 3-state_ECL; Then: Attach a 50 ohm resistor to the termination voltage ($V_{term} = VCC - 2 V$). Use this load to derive both the rising and falling edges.

If: The Model_type is either an Open_sink type or Open_drain type; Then: Attach either a 50 ohm resistor or the semiconductor vendor suggested termination resistance to either POWER or the suggested termination voltage. Use this load to derive both the rising and falling edges.

If: The Model_type is an Open_source type; Then: Attach either a 50 ohm resistor or the semiconductor vendor suggested termination resistance to either GND or the suggested termination voltage. Use this load to derive both the rising and falling edges.

c. Due to the resistor, output swings will not make a full transition as expected. However the pertinent data can still be collected as follows:

- 1) Determine the 20% to 80% voltages of the 50 ohm swing.
- 2) Measure this voltage change as "dV".
- 3) Measure the amount of time required to make this swing "dt".

d. Post the value as a ratio "dV/dt". The simulator extrapolates this value to span the required voltage swing range in the final model.

e. Typ, Min, and Max must all be posted, and are derived at the same extremes as the V/I tables, which are:

Ramp rates for CMOS models:

typ = typical voltage, typical temp deg C, typical process

min = minimum voltage, max temp deg C, typical process, minus "Y%"

max = maximum voltage, min temp deg C, typical process, plus "Y%"

Ramp rates for bipolar models:

typ = typical voltage, typical temp deg C, typical process

min = minimum voltage, min temp deg C, typical process, minus "Y%"

max = maximum voltage, max temp deg C, typical process, plus "Y%"

where nominal, min, and max temp are specified by the semiconductor vendor. The preferred range is 50 deg C nom, 0 deg C min, and 100 deg C max temperatures.

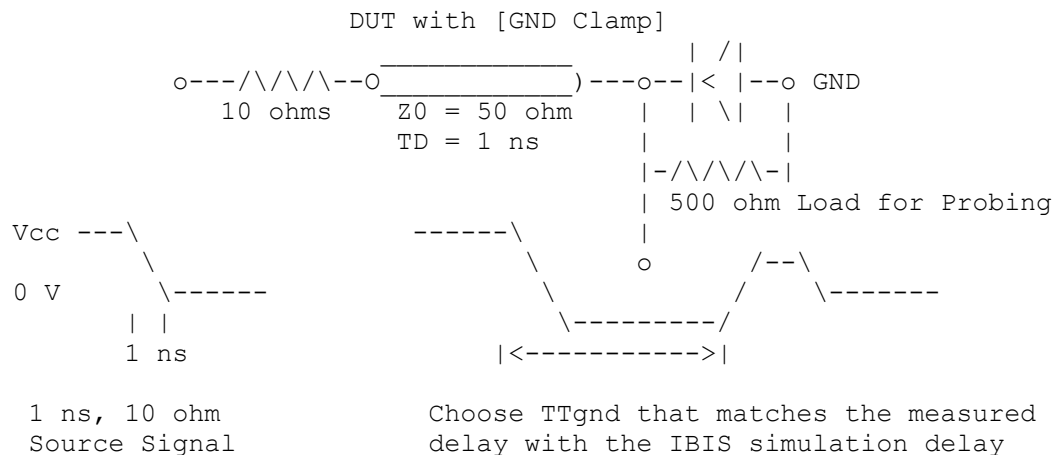
Note that the derate factor, "Y%", may be different than that used for the V/I table data. This factor is similar to the X% factor described above. As in the case of V/I tables, temperatures are at the junction. During the IV measurements, the driving waveform should have a rise/fall time fast enough to avoid thermal feedback. The specific choice of sweep time is left to the modeling engineer.

4) Transit Time Extractions:

The transit time parameter is indirectly derived to be the value that produces the same effect as that extracted by the reference measurement or reference simulation.

The test circuit consists of the following:

- a) A pulse source (10 ohms, 1 ns at full duration ramp) or equivalent and transitioning between Vcc and 0 V,
- b) A 50 ohm, 1 ns long trace or transmission line,
- c) A 500 ohm termination to the ground clamp reference voltage for TTgnd extraction and to the power clamp reference voltage for TTpower extraction (to provide a convenient, minimum loading 450 ohm - 50 ohm divider for high-speed sampling equipment observation of the component denoted as the device under test), and
- d) The device under test (DUT).



Example of TTgnd Extraction Setup:

The TTgnd extraction will be done only if a [GND Clamp] table exists. A high to low transition that produces a positive "glitch", perhaps several nanoseconds later indicates a stored charge in the ground clamp circuit. The test circuit is simulated using the complete IBIS model with C_comp and the Ct model defined under the [TTgnd] and [TTpower] keywords. An effective TTgnd value that produces a "glitch" with the same delay is extracted.

Similarly, the TTpower extraction will be done only if a [POWER Clamp] table exists. A low to high transition that produces a negative "glitch", perhaps several nanoseconds later indicates a stored charge in the power clamp circuit. An effective TTpower value that produces a glitch with the same delay is extracted.

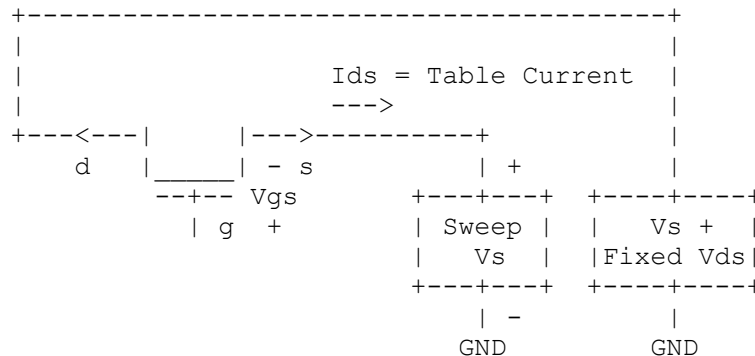
It is preferred to do the extractions with the package parameters removed. However, if the extraction is done from measurements, then the package model should be included in the IBIS based simulation.

5) Series MOSFET Table Extractions:

An extraction circuit is set up according to the figure below. The switch is configured into the 'On' state. This assumes that the Vcc voltage will be applied to the gate by internal logic. Designate one pin of the switch as the source node, and the other pin as the drain node. The Table Currents designated as Ids are derived directly as a function of the Vs voltage at the source node as Vs is varied from 0 to Vcc. This voltage is entered as a Vgs value as a consequence of the relationship:

$$V_{\text{table}} = V_{\text{gs}} = V_{\text{cc}} - V_{\text{s}}$$

V_{ds} is held constant by having a fixed voltage V_{ds} between the drain and source nodes. Note, $V_{ds} > 0$ V. The current flowing into the drain is tabulated in the table for the corresponding V_s points.



Example of Series MOSFET Table Extraction

It is expected that this data will be created from semiconductor vendor proprietary silicon models, and later correlated with actual component measurement.

Three methods of obtaining the data are covered next. They are:

- Using the data sheet.
- Using SPICE simulation.
- Using direct measurement.

These methods are not mutually exclusive and can be used to complement each other nicely. The most common (by far) method is to use the data sheet to find out the type of I/O cell connected to each pin and SPICE simulation to generate the behavioral curves for the I/O cells. Each method has its advantages and disadvantages.

- Using the data sheet.

The data sheet is particularly good for finding out which buffer types are connected to which pins, V_{ol} (max), etc. For example, V_{ol} (max) defines the worst case population limit on V_{ol} rather than an ideal, “typical” unit. The common practice in the semiconductor industry is to “guard band” V_{ol} (max) and similar properties since they are more likely to guarantee their data sheet numbers. This can lead to overly conservative designs and differences with simulator results at times.

As of this writing: All data sheets have component name, manufacturer, pinout, V_{inl} , V_{inh} , V_{ol} , V_{oh} , voltage range, and temperature range. Most data sheets have model type, C_{comp} and testloads. Few data sheets have V-I curves, ramp rates and package RLC. No data sheets have pin mapping and v/t curves. But, the industry is rapidly changing.

- SPICE simulation.

Most likely, the semiconductor company has already used a SPICE simulator (or derivative) to model the corners of the process distribution for a device. That is probably how they obtained the un-guardbanded V_{ol} (max) to begin with. Running enough units, measuring and characterizing them simply takes too long and costs too much. Certainly, if the semiconductor company has provided an IBIS model they have used a SPICE simulator to generate the beyond-the-rails

V-I behavior and any V-T curves included. It’s rare to see such data on a data sheet.

- Direct measurement.

Direct measurement is a great reality check. You never know what errors of omission or commission could

have crept into the data sheet or SPICE model. Don't mislead yourself into assuming that the units you will measure are from the center of the semiconductor supplier's distribution.

There are certain methods that run throughout these properties and their measurement or modeling. A V-I curve can be measured or simulated. In either case, by slowly ramping a voltage source at the buffer pin and measuring the resultant current. Being familiar with each description below will complement your understanding of the process.

You should understand that high speed digital rise/fall measurements are a sophisticated science in themselves. If you are going to do such measurements you will need a sampling scope with at least a 4 GHz bandwidth and a probe with less than a pF of loading capacitance.

The required "typ" column for all data represents typical operating conditions. For most [Model] keyword data the "min" column represents slow, weak performance and the "max" column represents fast, strong performance. Slow, weak and fast, strong usually refers to units of the device population that present those characteristics. Measured units or simulation projections based on models can be used.

The temperature and voltage should be varied in a manner where they amplify the slow, weak performance and the fast, strong performance. This way the "worst case" performance corners get defined. Note that not all technologies respond the same to variations in temperature and voltage with respect to slow, weak and fast, strong performance. For instance, the "min" column for TTL and ECL will contain the lowest temperature and for CMOS it will contain the highest temperature. IBIS itself sets up some default definitions for TYP-MIN-MAX for V-I curves:

For CMOS devices:

Typ = typical voltage, temperature (°C) and process.

Min = minimum voltage, maximum temperature and typical process minus x %.

Max = maximum voltage, minimum temperature and typical process plus x %.

For Bipolar devices:

Typ = typical voltage, temperature (°C) and process.

Min = minimum voltage, minimum temperature and typical process minus x %.

Max = maximum voltage, maximum temperature and typical process plus x %.

Default temperature definitions are: typ = 50°C, min = 0°C and max = 100°C.

7.2. Curves and Other Behavioral Data: Data Sheet Method

V-I Curves

Pullup and Power Clamp data refers to the high state operation of an output buffer. Pullup curves in a data book plot V_{oh} Vs I_{oh} . Power Clamp data is the plot of clamping diode V_{oh} Vs clamping diode current.

Pulldown and Ground Clamp data refers to the low state operation of an output buffer. Pulldown curves in a data book plot V_{ol} Vs I_{ol} . Ground Clamp data is the plot of clamping diode V_{ol} Vs clamping diode current.

The databook output V-I curves may be the total output current. The pullup/pulldown currents may not be separated out from their respective diode clamp currents when presented in a data book. These different elements must be separated out to enter the data into an IBIS format.

Input V-I curves do not exist for most parts unless there are clamping diodes on the input. This is because most parts have very high input impedances.

When taking V-I data off the curves, choose the points to save yourself labor in their linear portions - more widely spaced points - and add extra points in any knee areas. The curves must be monotonic for IBIS. That is, only one current can be used for each voltage point. You may have to do some data smoothing on occasion.

Some databooks provide a family of V-I curves taken under MIN-TYP-MAX conditions or various points in-between. All the better for entering worst case data in IBIS. The voltage range for the V-I curves covers $-V_{cc}$ to $+2V_{cc}$.

You will have to remember to enter the data in columns in the order:

Voltage – Typ – Min – Max

Left-to-Right when using a text editor to create the file.

Secondly, the databook voltage needs to be translated to the IBIS voltage.

For Pullup and Power Clamp this is:

$$V_{pullup}(IBIS) = V_{reference} - V_{oh}$$

Where $V_{reference}$ is the V_{cc} rail and V_{oh} is being swept over $-V_{cc}$ to $+2V_{cc}$.

For example, with $V_{cc} = 5V$:

$V_{oh}(V)$	$V_{pullup}(V)$
-5.0	10.0
0.0	5.0
10.0	-5.0

For Pulldown and Ground Clamp this is:

$$V_{pulldown}(IBIS) = V_{ol} - V_{reference}$$

Where $V_{reference}$ is the ground rail and V_{ol} is being swept over $-V_{cc}$ to $+2V_{cc}$.

For example, with $V_{gnd} = 0V$:

$V_{ol}(V)$	$V_{pulldown}(V)$
-5.0	-5.0
0.0	0.0
10.0	10.0

For standard ECL parts things are different. $V_{\text{reference}} = 0V$ is used for both pullup and pulldown. Therefore:

$$V_{\text{pullup}} = 0 - V_{\text{oh}} = -V_{\text{oh}}$$

$$V_{\text{pulldown}} = V_{\text{ol}} - 0 = V_{\text{ol}}$$

And, ECL devices always source (negative sign) current.

Many older datasheets do not cover the full $-V_{\text{cc}}$ to $+2V_{\text{cc}}$ range needed for signal integrity simulations. Assume the curves are linear in this extended range as an approximation to get the needed data points and extrapolate them. Do the clamp curves separately, but be sure you know where the diode knees are.

The current into a device (sink) is always positive and the current out of the device (source) is always negative by convention.

Note that even in the latest SPICE model, BSIM3, diode resistance is not properly accounted for. It is quite common to see SPICE simulated (for signal integrity applications) clamp curves with **giga-amps** or more of current at the voltage extremes. Obviously, this does not exist in reality. Note that the most common unit of current magnitude is milliamps. At the other extreme, you may see **.05 milliamps** or less. Use some judgement. Most of the time these numbers can be approximated to zero.

V-T Curves

It is rare to get a full-blown V-T curve in a data sheet. Therefore, I'm going to defer a full discussion of them to the SPICE Simulation and Direct Measurements section. If you do get such curves in the databook, use the ideas presented above to guide you. For example, the frequency of data points near knees Vs linear portions of the curve.

There is a whole discussion for when you need V-T curves as opposed to rise/fall times in our "How to Use the IBIS Model." It has to do with the added accuracy that is at times needed.

You will, most likely, get rise and fall time measurements on the data sheet that you can use directly and you are done. Provided – you understand what definition the semiconductor supplier has used for taking the data. Make any necessary translation to the IBIS definition of 20 % to 80 % of the (well behaved) output swing.

7.4. Curves and Other Behavioral Data: SPICE Simulation Method

Simulation Conditions

You may not get a SPICE model from the semiconductor supplier. After all, one of the two or three chief reasons that the IBIS spec was created was that semiconductor suppliers are unwilling to provide SPICE models! Assuming however, that you have one you can get started generating the IBIS behavioral curves. Rarely, when you get the SPICE model will you also get MIN-TYP-MAX parameter data with it also. Here is what to do:

You can put in estimates of the +/- variation from the typical or nominal values of the SPICE model elements and simulate under those conditions to get MIN-TYP-MAX data. Most often what I do is:

1. Simulate the V-I and V-T curves.
2. Consult with the semiconductor supplier to get a sense of how much their process varies.
3. Most often go +/- 10 % on the current for the V-I MIN-MAX curves and +/- 25% on the time for the V-T MIN-MAX curves.

V-I Curves

To start, use typical process parameters. To get pullup/pulldown curves for a buffer:

Set the control/enable inputs to turn on/off each pullup and pulldown device as required to go to output logic high and low.

Set the SPICE simulator for a DC sweep analysis. This is done by connecting a voltage source to the output node, sweeping it over $-V_{cc}$ to $+2V_{cc}$ and measuring the current into/out of the output node. Output clamp diodes, when present, must be disconnected in the SPICE model to obtain the pullup/pulldown curves. Next, reconnect the diodes and re-simulate to get the total turn on / turn off V-I curves. After you subtract out the pullup / pulldown portion you will be able to extract the clamp curves for inclusion in the IBIS file.

Most of the time you are going to simulate MIN-MAX curves as well as TYP. Let us say that the MIN voltage range is the same as the TYP voltage range minus 5 %. Then, adjust the sweep voltage range by the same amount when you run the simulation.

V-T Curves

As above: To start, use typical process parameters. To get rise/fall waveforms for an output buffer: Set the control/enable inputs to turn on/off each pullup and pulldown device as required to go to output logic high and low. Refer to the IBIS spec for specifying the output load or test fixture you will be driving.

Set the SPICE simulator for a transient analysis. Connect a voltage supply to the output node of V_{cc} . Remember to reconnect any output clamp diodes in the SPICE model if you disconnected them to obtain the pullup/pulldown curves.

Suppose this is a single discrete transistor you are modeling. Then you will drive the SPICE model input with a pulse waveform having a rise/fall time at least as fast (but, not a lot faster) as the fastest expected rise/fall time of the device being simulated. Also, the amplitude of the input drive should be enough to drive from hard on to hard off and vice versa. Most of the time you will be modeling the output buffer of an IC. Use the inherent internal process rise/fall time for the driver as provided by the semiconductor supplier.

The simulated rise/fall time is supposed to be the rise/fall of the buffer itself. So, remove internal pin/package parasitics from the SPICE model before running the simulation. Else, remember to use the V-T data at the internal die connection point node in the IBIS file.

Remember to connect the load to the proper rail when running the simulations. Let us say you are using a standard $50\ \Omega$ load. On pullup connect it to the V_{cc} rail and on pulldown connect it to ground, as appropriate. For open pullup or pulldown devices and ECL use the load and voltage used by the semiconductor supplier when they specified propagation delays.

Remember that the rise/fall slew rate interval for IBIS is 20 % to 80 % of the normal output swing if you are only going to use ramp rate information instead of full V-T data. Remember that serious ringing and non-monotonicities tend to invalidate your simulations because they are hard to interpret, repeat, reproduce and verify with bench measurements. You want clean output waveforms for good model data.

Most of the time you are going to simulate MIN-MAX curves as well as TYP. Let us say that the MIN voltage range is the same as the TYP voltage range minus 5 %. Then, adjust the sweep voltage range by the same amount when you run the simulation.

7.5. Curves and Other Behavioral Data: Direct Measurement Method

Setup

To obtain or verify behavioral curves from measurement data you will need a proper lab setup. Most high speed digital logic is Electro Static Discharge (ESD) sensitive. So, set up your lab procedures and handle the devices accordingly.

You will need:

- A programmable power supply capable of sourcing and sinking the required current over the range of $-V_{cc}$ to $+2V_{cc}$. The output must be floating.
- A curve tracer.
- A digital sampling oscilloscope with at least 4GHz of bandwidth and a high impedance, low capacitance probe. This usually means an active FET probe with $C_{in} \leq 1pF$.
- A DC test fixture.
- An AC rise/fall test fixture.
- A thermoelectric hot/cold plate or probe to control die temperature for MIN-MAX data.

V-I Curves

Mount the device under test (DUT) in the DC test fixture to measure the V-I curves. Connect the power and ground pins of the fixture to the programmable power supply. Attach the hot/cold probe to the DUT with a very thin layer of thermal grease. Adjust the temperature of the DUT as appropriate. Provide enough time for the die to stabilize if you are going to be adjusting its temperature.

Connect the curve tracer to the appropriate output pin in the appropriate state, high or low, and use it to trace (measure) the V-I characteristic of that buffer.

The curve tracer may not be able to sweep the entire range of $-V_{cc}$ to $+2V_{cc}$ of the DUT. You may need to extrapolate the data to cover the required range. Indeed, by sweeping that entire range you may exceed the device's recommended absolute maximum or minimum currents. It is recommended, however, to turn on any clamp diodes and sweep out to the range of the absolute maximum and minimum currents.

Most simulators extrapolate the last two data points in a table to calculate values beyond the table's range. Make sure that all curves going to zero (or any other constant value) have at least the last two data points as zero (or any other constant value). Reference pullup and power clamp voltages to V_{cc} and remember that current into the DUT is positive and out of is negative by convention.

V_{cc} – relative pullup and power clamp V-I data can be obtained directly. Connect the curve tracer's negative (reference) lead to V_{cc} of the DC test fixture and set the curve tracer for negative sweep. Make sure no DC ground path connects back through the curve tracer and the power supply and device grounds and watch out for polarized capacitors.

For pulldown and ground clamp data you will be referencing the curve tracer to ground and sweeping it in the positive direction. But, you will still have to insure the supply is floating.

Buffers with built-in active ramp rate and time delayed feedback circuitry can produce anomalous results for both V-I and V-T curves. Always consult with the semiconductor supplier when modeling such devices. When you are measuring a buffer's V-I curve, if there are output clamps present, the clamp currents are combined with the pullup

/ pulldown currents. In the case of a 3-state output, the device can be put into its high impedance output (open collector) state and will produce the V-I curves for the clamps alone allowing you to separate out the pullup / pulldown portions.

It is assumed that all simulators sum the currents of the pullup and/or pulldown curves and the appropriate clamps when present.

Non 3-stated devices must be handled differently because the clamp curves cannot be separated out in an enabled output with lab measurements alone. The pullup and pulldown curves can contain the sum of the clamping characteristics and the output structure. The clamping curves must contain all zeroes or the clamping curve keywords must be omitted in this case.

V-T Curves

Mount the device under test (DUT) in the AC test fixture to measure the V-T curves. Connect the power and ground pins of the fixture to the programmable power supply. Attach the hot/cold probe to the DUT with a very thin layer of thermal grease. Adjust the temperature of the DUT as appropriate. Provide enough time for the die to stabilize if you are going to be adjusting its temperature.

In these measurements you will be measuring the rising and falling switching waveforms of the DUT as it switches. My chief assumption is that you will be modeling extremely fast switching devices with edge rates of a couple of nanoseconds or less. Ordinary probe ground leads of 6 inches won't do. You will have to keep them to ½ inch or less. Plus, using a very low capacitance FET probe means you will have to follow ESD procedures in handling the sampling scope instrumentation to say nothing of the DUT. As well, you will have to know something of high speed layout and shielding in your AC fixture design and construction.

The rise and fall waveforms that you measure at the output pins of the device will include its pin / package parasitics. To extract the behavior of the bare die (per the IBIS philosophy) will require the application of some de-embedding technique.

Finally, a note of caution: It can be difficult to switch any given output on a complex state machine. And, circuits with output ramp rate control feedback (i.e., non-simple) such as GTLP can be very difficult to measure correctly. Measured IBIS model accuracy works best on simple devices.

7.6. Field Solver and TDR Measurements: RLGC

RLGC Matrices Illustrated

RLGC matrices in IBIS are broken out into their constituent R, L, G and C matrices. It is left to the simulator company to recombine them in an appropriate manner. Most of the time the G elements are so small that this matrix is set to zero.

To illustrate the appearance of a full, banded and banded symmetric matrix consider a 6 pin C matrix for illustration:

The main diagonal elements - C_{11} C_{22} - - - are the self capacitances of the pins to ground.

The off - main diagonal elements - C_{12} C_{13} - - - are the mutual capacitances of pins 1 to 2, 1 to 3, - - -.

Full Matrix

C_{11}	C_{12}	C_{13}	C_{14}	C_{15}	C_{16}
C_{21}	C_{22}	C_{23}	C_{24}	C_{25}	C_{26}
C_{31}	C_{32}	C_{33}	C_{34}	C_{35}	C_{36}
C_{41}	C_{42}	C_{43}	C_{44}	C_{45}	C_{46}
C_{51}	C_{52}	C_{53}	C_{54}	C_{55}	C_{56}
C_{61}	C_{62}	C_{63}	C_{64}	C_{65}	C_{66}

Usually, the subscript index, C_{ij} , is a rough indicator of distance. The greater the ij difference the farther apart the pins are. Mutual parasitics also fall off rapidly with separation. So, many elements can be approximated to zero and eliminated from the matrix, leading to:

Banded Matrix (band of 3)

C_{11}	C_{12}	C_{13}	-	-	-
C_{21}	C_{22}	C_{23}	C_{24}	-	-
C_{31}	C_{32}	C_{33}	C_{34}	C_{35}	-
-	C_{42}	C_{43}	C_{44}	C_{45}	C_{46}
-	-	C_{53}	C_{54}	C_{55}	C_{56}
-	-	-	C_{64}	C_{65}	C_{66}

Most packaging mediums are homogeneous and isotropic within the volume of interest. This means that the capacitance from pin 1 to pin 2 is equal to the capacitance from pin 2 to pin 1. The rules of matrix algebra say that we can simplify a symmetric matrix by eliminating all the elements below (or above, but not both) the main diagonal, leading to:

Banded Symmetric

C_{11}	C_{12}	C_{13}	-	-	-
-	C_{22}	C_{23}	C_{24}	-	-
-	-	C_{33}	C_{34}	C_{35}	-
-	-	-	C_{44}	C_{45}	C_{46}
-	-	-	-	C_{55}	C_{56}
-	-	-	-	-	C_{66}

Field Solver

In this section, as well as the next, we present information that is more a discussion of what semiconductor suppliers can do in IBIS modeling than what end users of devices can do in IBIS modeling.

Electromagnetic field solver software can extract the electrical pin/package parasitic parameters of an IC device. The input required is a mechanical model/drawing of the packaged device, its lead frame, wire bonds, etc.

A customer of the semiconductor supplier can hardly ever expect to receive such proprietary information. Therefore, the customer is usually reduced to asking the semiconductor supplier for the data on the electrical pin/package parasitic parameters of the IC device they wish to model. That course of action is my recommendation to you.

TDR-LCR Measurements

Time Domain Reflectometry (TDR) sampling oscilloscopes and Inductance-Capacitance-Resistance meters (LCR) can be used to measure the electrical pin/package parasitic parameters of an IC package. However, two things are difficult for a customer to do.

First, a user receives a complete device including the IC. Thus, what they would measure includes the loading of the device. It is difficult to separate out the package properties themselves from this measurement. Especially, since they cannot usually make measurements directly on the die itself. Second, the measurement of mutual pin-pin parasitics is difficult in and of itself. It is next to impossible to make these measurements with the die also hooked up.

Worst-case you can purchase a number of units of the device you intend to characterize package parasitics for and destroy them for that purpose. The TDR method involves placing opens and shorts at the position where the die would normally be connected.

The semiconductor supplier will often make TDR-LCR measurements of electrical pin/package parasitic parameters on a set of “dummy” devices. Particularly, this is done to verify field solver results and calibrate physical parameters used in the simulation. This dummy device is a bare leadframe without the die. The dummy device(s) may include “routed” (but unconnected) wirebonds and encapsulating materials and just the bare leadframe itself.

A customer of the semiconductor supplier can hardly ever expect to receive such a dummy package for characterization measurements. Therefore, the customer is usually reduced to asking the semiconductor supplier for the data on the electrical pin/package parasitic parameters of the IC device they wish to model. That course of action is my recommendation to you.

Visit the following web sites for further information on TDR instruments, measurements and interconnect characterization:

HP Test & Measurement – instruments.

<http://www.tmo.hp.com>

TDA Systems – software drivers and TDR applications for HP and Tektronix instruments.

<http://www.tdasystems.com>

Tektronix Test & Measurement – instruments.

<http://www.tek.com/Masurement/>

8. IBIS Model File Generation

The formal IBIS standard, latest released version, should be referred to in constructing the actual IBIS model file. It goes into great detail on syntax and how to construct the file. The specification, at least v2.1, is not well organized for finding syntax and file construction rules. Therefore, I have prepared “**Appendix A: IBIS Model Syntax**” and attached it to the end of this file.

This author strongly urges the use of the IBIS “Golden Parser” during file construction on a check as you build basis. This is a free software program available from the IBIS Open Forum that will check for correct syntax and the presence of required model elements. It is available from:

<http://www.eia.org/eig/ibis/tools.htm>

Be sure you choose the correct version, DOS or UNIX, for your platform. After downloading and installing this program run it on the model file by typing at the prompt where the file is found:

```
ibis_chk <filename>
```

An example IBIS model file is attached (with the permission of Fairchild Semiconductor, Inc.) after Appendix A.

9. IBIS Visual Editors Available Free From Software Companies

As of this date, 1/19/99, there are some IBIS visual editors (GUIs) available free from some software companies.

From Cadence at:

http://www.cadence.com/software/pcb_info/pcb_software/spice.html

From HyperLynx at:

<http://www.hyperlynx.com/vis.ibis.html>

10. Common Mistakes and Their Correction

The IBIS Golden Parser catches syntax problems. But, it doesn't analyze the data and will miss the following mistakes. Fortunately, most of them are easy to catch visually.

1. Numerous [End] statements.

Improper use of SPICE2IBIS tools.

Correction: Textedit the IBIS file and remove the extra statements.

2. Syntax errors of all sorts.

For example: Tab characters following keywords, lines longer than 80 ASCII characters, non-ASCII characters, (/) \ % @ # * etc., etc. Data item names too many characters long. Missing keywords and data items. Literal (actual) keywords inserted in the text of un-commented-out notes. File names that are different than the [File Name] keyword. Etc.

Only spaces and underbars "_" are allowed in names.

Syntax errors in supplied IBIS models are so common as to hardly bear mentioning.

Correction: Use the latest version of the IBIS Standard, this 3Com IBIS Standard, the IBIS GoldenParser downloaded from their website and Appendix A: "IBIS Model Syntax Guide" to diagnose and fix the problem. Otherwise, have the IBIS model supplier send you a corrected file.

3. Missing units in [Package]. H instead of nH, F instead of pF.

Correction: Verify the correct units with the IBIS model supplier and textedit the IBIS model file to add them if the work isn't excessive. Otherwise, have the IBIS model supplier send you a corrected file.

4. No minus signs on current out of a device ([Pullup], [GND Clamp]).

Correction: Verify the correct current convention with the IBIS model supplier and ask them to send you a corrected model file. Because of the amount of work required, textedit the IBIS model file to correct the problem only if the supplier is not forthcoming in a timely fashion.

5. [Pullup] and [POWER Clamp] not Vcc relative.

Comment: The IBIS convention is $V_{table} = V_{cc} - V_{output}$. So, for a Vcc of 5 volts when:

$V_{output} = -5$, then $V_{table} = 10$

$V_{output} = 0$, then $V_{table} = 5$

$V_{output} = 10$, then $V_{table} = -5$

Correction: Verify the correct voltage convention with the IBIS model supplier and ask them to send you a corrected model file. Because of the amount of work required, textedit the IBIS model file to correct the problem by adding or subtracting a constant amount (usually the Vcc value) only if the supplier is not forthcoming in a timely fashion.

6. Range of V-I curves do not correspond to -Vcc to +2Vcc.

Correction: Verify the correct voltage range with the IBIS model supplier and ask them to send you a corrected model file. Because of the amount of work required, textedit the IBIS model file to correct the only if the supplier is not forthcoming in a timely fashion. You can add or subtract data points. Linear extensions of curves are reasonable when adding points

7. No clamps in [Model] – possible, but suspicious.

One possible explanation of missing clamp curves is that their currents were included in the pullup/pulldown curves of a measured device model. Particularly in a non tri-state-able device where they cannot be separated out of the total output current. Another possible explanation is a "5 volt TTL compatible" input on a low voltage device where they are not present. But, most high speed digital devices incorporate ESD protection.

Correction: After verifying problem, require generation of a corrected model by model supplier. Otherwise not correctable.

8. Unrealistic currents in clamp curves, i.e., GigaAmperes, Nano-Picoamperes, etc.

Correction: Consult with device supplier regarding realistic maximum and minimum currents. Contact model supplier and ask them to send you a corrected model file. Because of the amount of work required, textedit the IBIS model file to correct the problem only if the supplier is not forthcoming in a timely fashion.

To correct the file, delete all the unrealistically high data entries. Also, clamp curves should eventually **clamp**. Instead of ridiculously small values at the end of the curve, just set the current to zero. Most simulators want to see at least two consecutive sets of 0mA at the end of all clamp curves.

9. Non-unique [Model] statements, i.e., two cells called “Output.”

Correction: Consult with device supplier regarding which cells are the correct ones. Contact model supplier and ask them to send you a corrected model file. Textedit the IBIS model file to correct the problem only if the supplier is not forthcoming in a timely fashion. To correct the file, delete all the incorrect cells.

10. [Ramp] dt doesn't represent 20% to 80% into 50 ohms.

Correction: Get the corrected slew rates from the model supplier and textedit the IBIS model file to correct the problem. If the supplier is not forthcoming in a timely fashion, do the following:

The slew rate you have, dV/dt_{original} , will have to be “resized” to the correct definition of 20% to 80% of the output switching range.

First, you will have to establish the correct output switching range, call this ΔV . Most often this will be $V_{cc} - 0$ volts. But, not always. For instance, the output swing of a BTL driver is 2.1 to 1.1 volts or 1 volt.

Then, calculate 60% (80% - 20%) of $\Delta V = dV_{\text{new}}$.

Next, find dt_{new} given that $dV/dt_{\text{original}} = dV/dt_{\text{new}}$.

Finally, enter the corrected slew rate(s) in the IBIS file.

11. Slew Rates ([Ramp] - dV/dt_r , dV/dt_f) are ridiculous, i.e. 1.5E-10nS.

Comment: What can I say?

Correction: You get the idea.

12. Data table typ-min-max in wrong order.

Correction: Contact model supplier and ask them to send you a corrected model file. Because of the amount of work required, textedit the IBIS model file to correct the problem only if the supplier is not forthcoming in a timely fashion. To correct the file, all the data will have to be re-entered in the correct order.

13. Big discontinuities (large spikes) and non-monotonicity in V-I or V-T curves when viewed visually.

Comment; Most simulators nowadays can handle small discontinuities in the input data fed them. But, large discontinuities usually prevent convergence. Large discontinuities are also not realistic and are usually caused by measurement artifacts and/or simulation of unrealistic models.

The IBIS golden parser, *ibischk2* (and probably many other versions), checks for non-monotonicity in the IBIS file and gives warnings. Any non-monotonicity data can be removed when the parser gives a warning.

Correction: Again, contact the model supplier and ask them to send you a corrected model file. Because of the amount of work required, textedit the IBIS model file to correct the problem only if the supplier is not forthcoming in a timely fashion. To correct the file, delete all the unrealistic data entries and re-enter *smoothed* data for the offending points.

14. Double counting of clamp currents, i.e., [GND Clamp] magnitudes in both [GND Clamp] and [Pulldown].

Comment: The V-I curves of an output, as measured, will include the action of the pullup/pulldown curves and the clamps, if present. In many devices it is possible to disable the pullup/pulldown and then measure the action of the clamps alone. Sometimes model suppliers forget to subtract the clamp currents from the total output behavior and present the behavior of the pullup/pulldown itself.

Correction: contact the model supplier and ask them to send you a corrected model file. Because of the amount of work required, textedit the IBIS model file to correct the problem only if the supplier is not forthcoming in a timely fashion. To correct the file, subtract the clamp currents from the total output currents and enter the remainder as the pullup/pulldown curve(s).

15. Common Differential Pin-Pair Mistakes:

Making the non-inverting pin inverting, or vice versa, on drivers or receivers.

Entering Launch Delay data for a receiver (Input) cell.

Entering Vil or Vih data for a driver (Output) cell.

11. IBIS Model Verification and Approval Levels

11.1. Definitions

3Com has four levels of verification and approval:

Level 1	by direct measurement: High level of approval.
Level 2	by correlation with a correlated SPICE model.
Level 3	by correlation with a data sheet.
Level 4	No parametric verification - will run in simulator: Low level of approval. IBIS model file checked for correct syntax with IBIS Golden Parser.

The process of achieving these levels of approval will next be discussed. This will be done in reverse order. That is, from level 4 to level 1.

11.2. Level 4 Approval: Syntax Correct and Reality Checks:

Golden Parser Syntax Check.

See the latest released IBIS spec for syntax rules for allowed line lengths, name lengths, allowed characters, etc. All IBIS model files get a .ibs file extension in their file names.

IBIS syntax rules are scattered throughout the text of the IBIS spec and are tedious to find, memorize and keep track of. The IBIS “**Golden Parser**” - current, past and future versions, are downloadable free in object code format for many platforms from:

ANSI/EIA-656 IBIS – Tools:

<http://www.eia.org/eig/ibis/tools.html>

To run the program go to the directory where the <filename.ibs> resides and at the prompt type:

```
ibis_chk <filename.ibs>
```

Be sure to download the latest version / version the IBIS file was created with to check your file with.

The Golden Parser source code is available from the EIA IBIS Committee for a nominal fee. It creates data structures from model data that simulators can use in addition to checking syntax. To obtain and learn about terms and conditions, contact:

EIA
2500 Wilson Blvd.
Arlington, VA 22201
703-907-7545
703-907-7501 - FAX

Check and correct common mistakes.

See the previous section; section 8, for a list of some common mistakes.

Do a reality check on V-T data.

When V-T data is given you can check for consistency with V-I data. Most often simulating a SPICE model into a resistive 50 ohm load generates this data. When you see the output voltage wander to, say 3.32 volts when the pullup resistor has been connected to a 3.3 volt supply, this is most likely a simulation artifact and not a real transistor level effect.

Also:

For a rising waveform (V-T data) at time 0 (zero) the current (V-I data) should exactly satisfy:

$$(V_{\text{out}} - V_{\text{fixture}}) / R_{\text{fixture}} = I_{\text{pulldown}} + I_{\text{powerclamp}} + I_{\text{gndclamp}}$$

where:

I_{pulldown} is defined for $V = (V_{\text{out}} - V_{\text{pulldown_ref}})$

$I_{\text{powerclamp}}$ is defined for $V = (V_{\text{out}} - V_{\text{powerclamp_ref}})$

I_{gndclamp} is defined for $V = (V_{\text{out}} - V_{\text{gndclamp_ref}})$

Similarly:

For a falling waveform (V-T data) at time 0 (zero) the current (V-I data) should exactly satisfy:

$$(V_{\text{out}} - V_{\text{fixture}}) / R_{\text{fixture}} = I_{\text{pullup}} + I_{\text{powerclamp}} + I_{\text{gndclamp}}$$

where:

I_{pullup} is defined for $V = (V_{\text{out}} - V_{\text{pullup_ref}})$

$I_{\text{powerclamp}}$ is defined for $V = (V_{\text{out}} - V_{\text{powerclamp_ref}})$

I_{gndclamp} is defined for $V = (V_{\text{out}} - V_{\text{gndclamp_ref}})$

Run simulations with test load in IBIS signal integrity simulator.

Many different simulations can be run in an IBIS signal integrity simulator as a reality check. Particularly, in the application where the model is intended to be used. For a full discussion of this applications oriented reality check see "How to Use the IBIS Model."

11.3. Level 3 Approval: Verify Model to Data Sheet

To verify a model against its data sheet is defined here to mean to verify the model against its inputted, primarily documented, data. The originator of the IBIS file should be able to supply you with copies of the documents they used.

Tables spelling out the possible sources of data use to construct an IBIS file are included in 3Com's "Creating an IBIS model." They are repeated here to show the types of document check sources you can expect to deal with:

Table 14: General Properties - refer to Table 1 for req./not req., definitions, etc.

Keyword	Sub Parameter	Most Likely Check Source	Alternate Source	Notes
[IBIS Ver]		IBIS 2.1		
[Comment Char]		IBIS 2.1		
[File Name]		Originator		
[File Rev]		Originator		
[Date]		Originator		
[Source]		Name of originator		
[Notes]		Originator		
[Copyright]		Originator		
[Disclaimer]		Originator		
[Manufacturer]		Datasheet		

Table 15: Component Properties - refer to Table 2 for req./not req., definitions, etc.

Keyword	Sub Parameter	Most Likely Check Source	Alternate Source	Notes
[Component]	Si_location Timing_location	Datasheet		
[Manufacturer]		Datasheet		
[Voltage Range]		Datasheet	Manufacturer	
[Temperature Range]		Datasheet	Manufacturer	

Table 16: Package & Pin Properties - refer to Table 3 for req./not req., etc.

Keyword	Sub Parameter	Most Likely Check Source	Alternate Source	Notes
[Package]	Rpkg, Lpkg, Cpkg	Datasheet		
[Pin]	signal_name, model_name, Rpin, Lpin, Cpin	Datasheet, Manufacturer	Field solver, network analyzer	
[Package Model]		Manufacturer		
[Define Package Model]				1
[Manufacturer]		Manufacturer		2
[OEM]		Manufacturer		
[Description]		Originator		
[Number of Pins]		Datasheet		
[Pin Numbers]		Datasheet		
[Number Of Sections]	Len, L, R, C, Fork, Endfork	Originator		

(Table 16 cont.)

Table 16 (cont.): Package & Pin Properties - refer to Table 3 for req./not req., etc.

Keyword	Sub Parameter	Most Likely Check Source	Alternate Source	Notes
[Model Data]				1
[Resistance Matrix]	Banded_matrix, Sparse_matrix, Full_matrix	Manufacturer	Field solver, network analyzer	
[Inductance Matrix]	Ibid	Ibid	Ibid	
[Capacitance Matrix]	Ibid	Ibid	ibid	
[Row]		Originator		3
[Bandwidth]		Originator		4
[End Model Data]		Originator		1
[Pin Mapping]	pulldown_ref, pullup_ref, gnd_clamp_ref, power_clamp_ref	Datasheet	Manufacturer	
[Rac]		Datasheet	Manufacturer	
[Cac]		Datasheet	Manufacturer	
[Rgnd]		Datasheet	Manufacturer	5
[Rpower]		Datasheet	Manufacturer	5
[Diff Pin]	inv_pin, vdiff, tdelay_typ, tdelay_min, tdelay_max	Datasheet	Manufacturer	
[Series Pin Mapping]	pin_2, model_name, function table_group	Datasheet		
[Series Switch Groups]	On, Off	Originator		

Table 17: V-I Properties -refer to Table 4 for req./not req., definitions, etc.

Keyword	Sub Parameter	Most Likely Check Source	Alternate Source	Notes
[Model]	Polarity, Enable, Vinl, Vinh, C_comp, Vref, Vmeas, Rref, Cref Model_type(s): Input, Output, I/O, 3-State, Open drain, Open_sink, I/O_open_sink, Open_source, I/O_open_source, Input_ECL, Output _ECL, I/O_ECL, Terminator, Series or Series_switch	Datasheet	Manufacturer	See figure 2
[On]		Datasheet	Manufacturer	
[Off]		Datasheet	Manufacturer	
[R Series]		Datasheet	Manufacturer	
[L Series]		Datasheet	Manufacturer	
[C Series]		Datasheet	Manufacturer	
[Rl Series]		Datasheet	Manufacturer	
[Rc Series]		Datasheet	Manufacturer	
[Lc Series]		Datasheet	Manufacturer	
[Series Current]		Datasheet	Manufacturer	
[Series MOSFET]		Datasheet	Manufacturer	

Table 17 (cont.): V-I Properties -refer to Table 4 for req./not req., definitions, etc.

Keyword	Sub Parameter	Most Likely Check Source	Alternate Source	Notes
3Com Requirement	Vol, Voh	Datasheet	Manufacturer	
3Com Requirement	Technology	Datasheet	Manufacturer	
[Pullup]		Datasheet, Manufacturer	SPICE simulation, measurement	
[Pulldown]		Datasheet, Manufacturer	SPICE simulation, measurement	
[GND Clamp]		Datasheet, Manufacturer	SPICE simulation, measurement	
[POWER Clamp]		Datasheet, Manufacturer	SPICE simulation, measurement	
[Pullup Reference]		Datasheet	Manufacturer	
[Pulldown Reference]		Datasheet	Manufacturer	
[GND Clamp Reference]		Datasheet	Manufacturer	
[POWER Clamp Reference]		Datasheet	Manufacturer	
[Model Selector]		Datasheet		
[Model Spec]	Vinh, Vinl, Vinh-, Vinh+, Vinl-, Vinl+, S_overshoot_high, S_overshoot_low, D_overshoot_high, D_overshoot_low, D_overshoot_time, Pulse_high, Pulse_low, Pulse_time, Vmeas	Datasheet		

(Table 17 cont.)

Data sheets can contain V-I characteristic curves in which case the V-I curves of the IBIS model can be verified against the data. However, you must remember to get your conventions on voltage correct. Remember:

The IBIS convention is $V_{\text{table}} = V_{\text{cc}} - V_{\text{output}}$ for pullup and powerclamp

The IBIS convention is $V_{\text{table}} = V_{\text{output}} - V_{\text{reference}} = V_{\text{output}} - 0$ (usually) $= V_{\text{output}}$ for pulldown and groundclamp

Table 17 (cont.): V-I Properties -refer to Table 4 for req./not req., definitions, etc.

Keyword	Sub Parameter	Most Likely Check Source	Alternate Source	Notes
[Add Submodel]	Mode (Driving, Non_Driving, All)	Datasheet		
[Submodel]	Submodel_type (Dynamic_Clamp, Bus_Hold)	Datasheet		
[Submodel Spec]	V_trigger_r, V_trigger_f, Off_delay	Datasheet		
[GND Pulse Table]		Datasheet		
[POWER Pulse Table]		Datasheet		
[TTgnd]	TT(typ), TT(min), TT(max)	Datasheet		
[TTpower]	ibid	Datasheet		

Table 18: V-T Properties - refer to Table 5 for req./not req., definitions, etc.

Keyword	Sub Parameter	Most Likely Check Source	Alternate Source	Notes
[Ramp]	dV/dt_r, dV/dt_f, R_load	Datasheet, Manufacturer	SPICE simulation, measurement	
[Rising Waveform]	R_fixture, R_dut, C_fixture, C_dut, L_fixture, L_dut, V_fixture, V_fixture_min, V_fixture_max	SPICE simulation, measurement	Datasheet, Manufacturer	See figure 3
[Falling Waveform]	Ibid	Ibid	Ibid	
[Driver Schedule]	Rise_on_dly, Rise_off_dly, Fall_on_dly, Fall_off_dly	Datasheet		

Table 19: Board Description Properties - refer to Table for req./not req., etc.

Keyword	Sub Parameter	Most Likely Check Source	Alternate Source	Notes
[Begin Board Description]				
[Manufacturer]		Datasheet	Originator	
[Number of Pins]		Datasheet	Originator	
[Pin List]		Datasheet	Originator	
[Path Description]		Datasheet	Originator	
[Reference Designator Map]		Datasheet	Originator	
[End Board Description]				
[End]				

11.4. Level 2 Approval: Correlate IBIS Model With SPICE Model

This verification amounts to a cross check between two simulations and it will be only a reality check unless the SPICE simulation has been correlated with measurements of actual devices or has otherwise established a history of credibility. That is, the SPICE model itself and/or the SPICE simulator can be inaccurate – a fact that neither the semiconductor suppliers nor the simulator software suppliers like to talk about.

The primary thing you will be doing will be to check the agreement between the waveforms from both simulators for a given virtual test case of a given virtual device modeled first in SPICE and then in IBIS.

There is a great advantage to using a cross check between and IBIS simulation and a SPICE simulation. Assuming that the original SPICE model (remember you want to verify the IBIS model) and both the IBIS and the SPICE simulators are all reasonably accurate you will be working in a very flexible medium. The printed wiring board (PWB) and devices you are using allow you to do “virtual breadboarding.” You don’t have to worry about damaging actual parts as you substitute (solder) in minimum, typical and maximum characteristic units. You don’t have to worry that the unit you are simulating has different measured properties than a real unit. And, its easy to “find” and simulate minimum, typical and maximum characteristic units, process corner units, worst case units, weighted population distribution samples or anything else you can imagine – literally. It’s just a matter of “what-if” on a simulator.

11.5. Level 1 Approval: Verify Model by Direct Measurement of Devices

For this section I am indebted to Peter LaFlamme of the EIA IBIS Subcommittee on IBIS Accuracy for material sent me on as yet to be released IBIS Accuracy Specification.

In verifying a model by direct measurement of devices we are at last addressing the verification of the accuracy of the model. The working definition of *accuracy* that we shall use is:

“The accuracy of a simulation is a measure of how close the result of the simulation comes to the true value.” In the case of behavioral modeling of high-speed digital circuits, the *true value* is what one accurately measures in the lab, and the behavioral simulation is a theoretical prediction. A highly accurate behavioral simulation is one in which the difference between simulation and lab data is small.

To further quote from the tentative spec:

The scope of the IBIS Accuracy Specification is based on IBIS keywords and sub-parameters, which in turn are based on the various features of I/O buffer behavior that the inventors of IBIS wanted to cover. Driven by the need to simulate more advanced I/O circuit designs, the list of features has grown considerably since the inception of IBIS. In order to accomplish something useful in a reasonable period of time with the resources available, the IBIS Accuracy Subcommittee decided to focus on the most fundamental of these features. The subcommittee chose to cover the IBIS keywords and sub-parameters that represent the behavior of the simple push-pull and open-drain drivers, as indicated by the Model_type sub-parameter of the Model keyword listed in the table below. The word "simple" loosely implies that the I/O circuit design does not employ feedback or any other form of edge rate or impedance control. An example of a circuit that is covered by the IBIS Accuracy Specification version 1.0 is the classic CMOS output buffer, which uses a PMOS pull-up and an NMOS pull-down. An example of a circuit that is *not* covered by this version of the specification is the original GTL output buffer (a la Bill Gunning), which employs a feedback network.

Two disclaimers are in order. First, package resistance and inductance are not easily measured on a sample component. While resistance and inductance measurements are not a direct part of this specification, the other measurements will introduce discrepancies when resistance or inductance is grossly amiss. Second, the methods defined by this version of the specification *may* be used with unspecified I/O buffers families, but the IBIS Accuracy Specification version 1.0 makes no attempt to insure coverage of their electrical behavior by the measurements and metrics defined within.

Table 19: IBIS Keyword and Subparameter Coverage

Keyword	Subparameter	Description
[Package]	C_pkg	Default package capacitance.
	L_pkg	Default package inductance.
	R_pkg	Default package resistance.
[Pin]	C_pin	Pin-specific package capacitance.
	L_pin	Pin-specific package inductance.
	R_pin	Pin-specific package resistance.
[Model]	C_comp	Capacitance associated with silicon.
	Model_type	Input, Output, I/O, 3-state, Open_drain.
[Pulldown]		Pull down IV curve.
[Pullup]		Pull up IV curve.
[GND_clamp]		Ground clamp IV curve.
[POWER_clamp]		Power clamp IV curve.
[Ramp]	dV/dt_f	Falling output edge rate measured at 20-80%.
	dV/dt_r	Rising output edge rate measured at 20-80%.

3Com will focus on the set of quantifiable and **measurable** (by a user as opposed to a supplier) parameters given in the keywords and sub-parameters:

Model_type, C_comp, Pullup, Pulldown, GND_clamp, POWER_clamp, Ramp, dV/dt_r, dV/dt_f,
Rising Waveform, Falling Waveform, vdiff and tdelay_typ.

- As found in the IBIS file being verified.

Parameters such as Pin Mapping are not proper subjects of an accuracy verification. They are pass/fail, right/wrong. Parameters too difficult for a user to verify: R_pin, C_pin, etc.: await the invention of enabling measurement techniques.

Parameters such as minimum V-I curve for Pullup are conditional on receiving a population distribution or process corner units from the vendor. These occurrences will be rare. Indeed, the units tested may not even be certifiably typical. What then to do? The method 3Com favors is to: (1) Simulate an *envelope* of response waveforms or parameter values; (2) Compare the measured data to fall within the envelope limits; (3) If individually measured units with model parameter values are received they can be measured and compared one-on-one with their simulated results.

Attached after Appendix A is the preliminary **“IBIS Accuracy Specification”** for reference only. Among the many interesting discussions are those regarding figures of merit for verification of accuracy.